D	Clock	Q	$\bar{Q}$	Comments
0	0	Q	$\bar{Q}$	Unchanged
1	0	Q	$\bar{Q}$	State
0	1	0	1	
1	1	1	0	

The D flip flop is used to store bits of binary numbers. Because it can be turned on or off by the clock, it is also used to catch or latch binary number present on the D input for a short time and store it on the Q and $\bar{Q}$ outputs. A D flip flop can be used as the output port of a micro-computer.

The symbol of the D flip-flop is shown below figure 6.29.

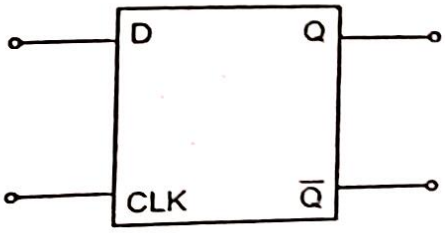


Figure 6.29

From the truth table, we can understand that when D is 0, the output is also zero. When the input is 1, the output is also 1. Hence it is called "DELAY FF" or "Buffer" or "Gated" D latch.

6.7 Basic of Counters

The counter has the ability to count and is a very important and useful subsystem of a digital system. A flip-flop can store one binary information. Hence, in order to store more binary information, we need registers. Registers are the one which is having a group of cascaded flip-flops.

A counter is a register. It is capable of counting the number of clock pulses, which have arrived at its clock input. So, it has to actually remember the number of clock pulses applied at the input.

The counters are used for counting pulses in large variety of counting applications such as control systems, computers, electronic and scientific instruments etc. There are wide range of applications of counters. It includes the occurence of events, frequency division, time sequence of operation of equipments of digital systems.

Counters can be broadly classified into the following two types

i) Asynchronous (or) Ripple (or) Serial counters

ii) Synchronous (or) Parallel counters.

A ripple counter is also called as an Asynchronous counter, because it is an asynchronous sequenctial circuit. But, Asynchronous counter is a synchronous sequential circuit. All the flip-flops in a synchronous counter are under the control of same clock pulse, which is synchronously applied to all the flip-flops. An asynchronous counter is not under the control of same clock pulse.

The comparison between the serial and parallel counters is given in the following table.

Serial Counters	*Parallel Counters*
Each FF is clocked by the by the previous FF	All the FFs are clocked simultaneously.
Propagation delay of the counter=propagation delay of each FFs × No.of FFs. Hence speed of operation is low.	Propagation delay of counter = propagation delay of one FF and the combinational hardware. Hence speed of operation is high.
Hardware is simple.	Hardware is more complex.

6.7.1 Ripple Counters

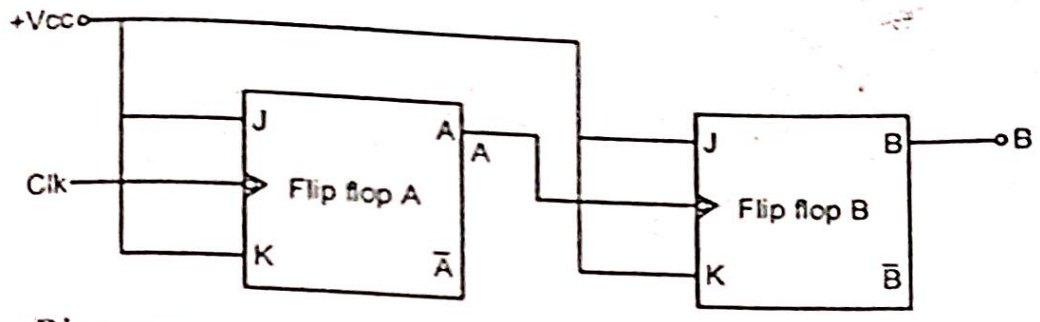
Consider a 2-bit binary counter. This should produce the count sequence as 0, 1, 2, 3. Two JK FFs are used. Both their inputs are connected to V_{cc}. Negative edge triggering is used here.

Now, the clock pulse comes in. Since both the inputs are connected HIGH, the FF-A toggles, during the negative going transition (NGT) of clock. This output of FF-A is the clock for FF-B. Hence FF-B also toggles during the NGT of FF-A.

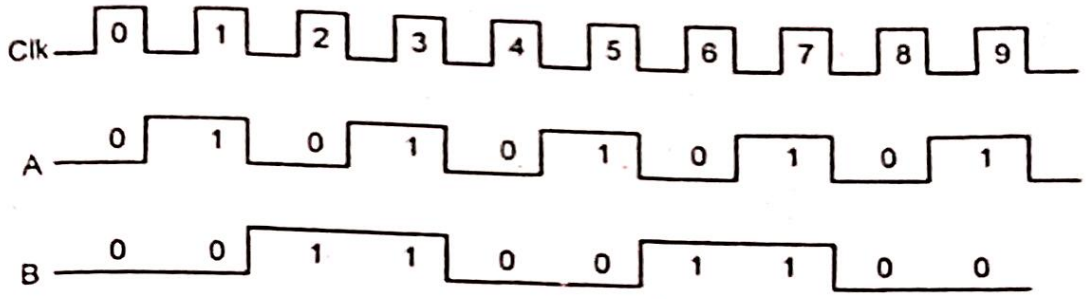
The timing diagram and the count table gives the count sequence of the counter. Each of these counts are said to be a "State" of a "plain 2-bit binary counter".

The counter circuit, timing diagram and the count table are shown in figure 6.30.

a) **Counter Circuit**



b) **Timing Diagram**



c) **Count Table**

Clk	*B*	*A*
0	0	0
1	0	1
2	1	0
3	1	1
4	0	0
5	0	1
6	1	0

Figure 6.30

After the counting finishes for 4 clock pulses, the sequences starts again. Hence for this reason, it is called "Modulo–4 counter". Modules of a counter is the total number of states of a counter.

We can notice that, 2 FFs can produce a modulo-4 (2^2) counter. So, far a modulo-8 counter 3 FFs ($2^3 = 8$) are required. Each FF depends on its predecessor for its clock. So the clock is said to be rippling through the flip-flops and the counter is called as Ripple or Asynchronous counters.

6.7.2 Up and Down Counters

We know counters can count up from 0 to 9. It is possible to make the counter count down by modifying the counters in any one of the 3 methods given below

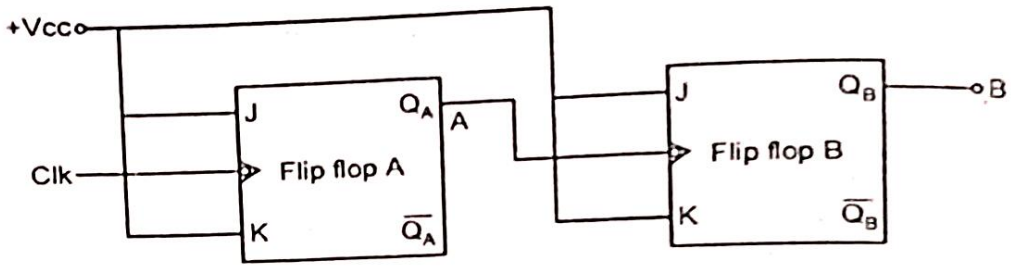
i) Make the FF to trigger on positive going transition (PGT) instead of NGT.

ii) Connect $\overline{Q}$ of one FF to the T of the next FF instead of Q.

iii) Take the counter outputs from $\overline{Q}$.

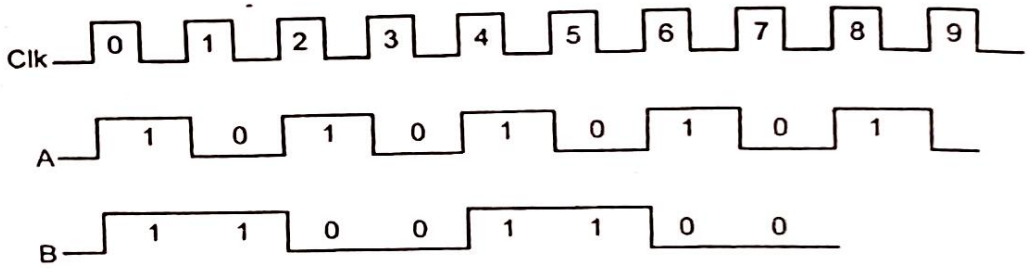
We can construct a modulo-4 down counter by using the above methods.

I - Method



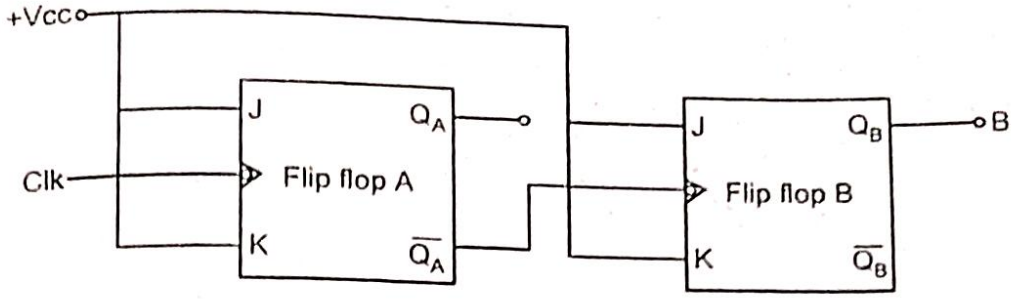
(a) Counter circuit

This is obtained by modifying the clock of the ripple counter.

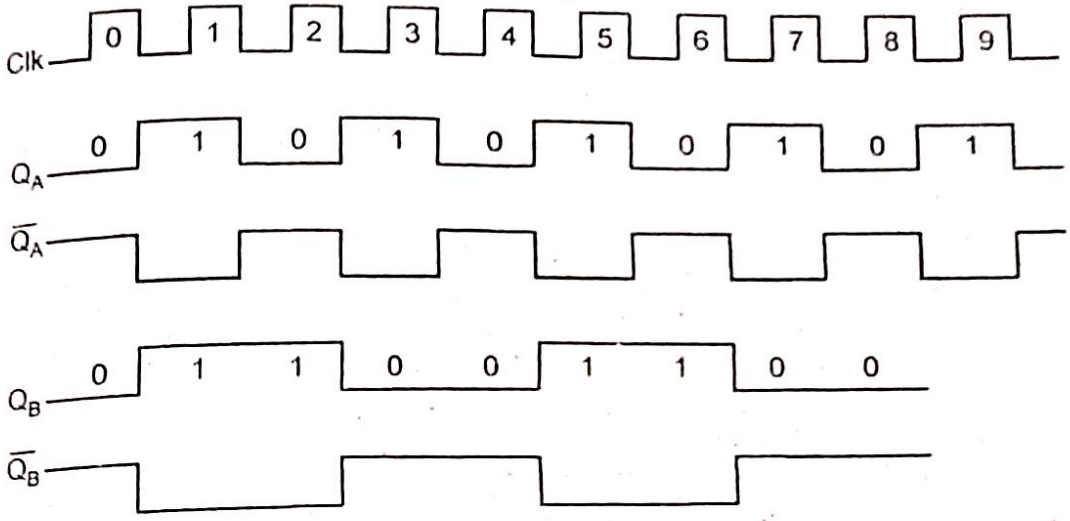


(b) Timing diagram

Method - 2



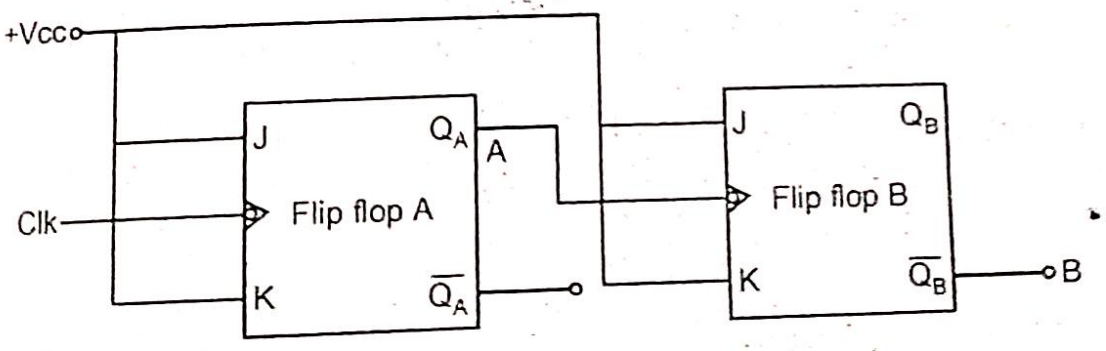
(a) Counter circuit



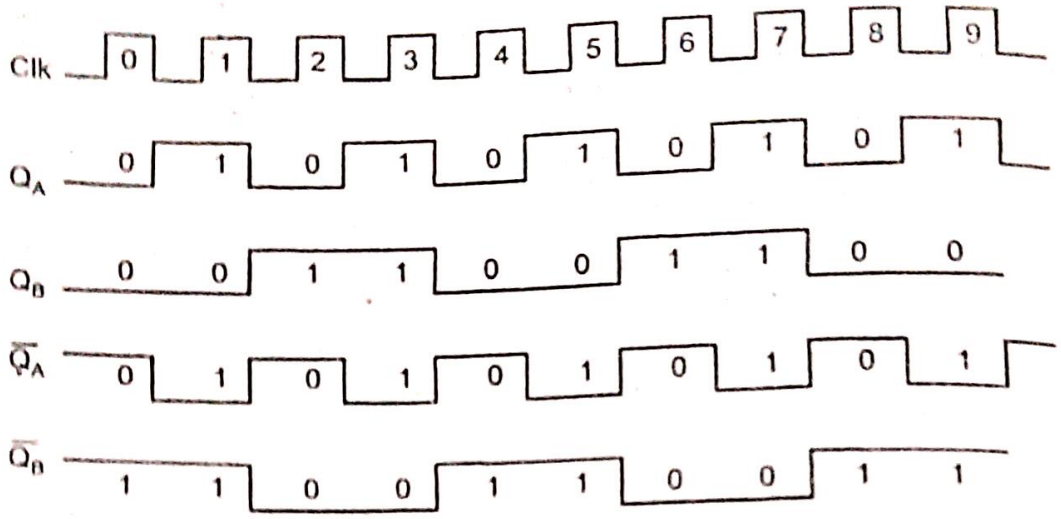
(b) Timing diagram

By using $\overline{Q_A}$ as clock pulse for the FF-B, and taking the counter outputs from Q_A Q_B, we obtain this.

Method - 3



(a) Counter circuit



(b) Timing diagram

Figure 6.31

This is obtained by taking the counters output from $\overline{Q}$. Hence it is clear that, if any one of these methods are used, we can convert an up-counter to a down counter.

6.7.3 Ring Counter

This counter is used to generate gating signals. This shifts a single 1 from its input the output. This is a serial transfer of information, where the bit stays on for a number of pulses equal to the number of bits in the shift registers. This type of generating "word time signals" is necessary in the control unit of serial computers.

Timing Sequence

For instance, if the word length of a computer is 8 bits, the output of the control unit should stay on for 8 clock pulses. So that start bit enables 3 bit counter which produces 8 states and for the 8 states the output of the control unit stays ON.

The logic diagram for word time control is shown in figure 6.32.

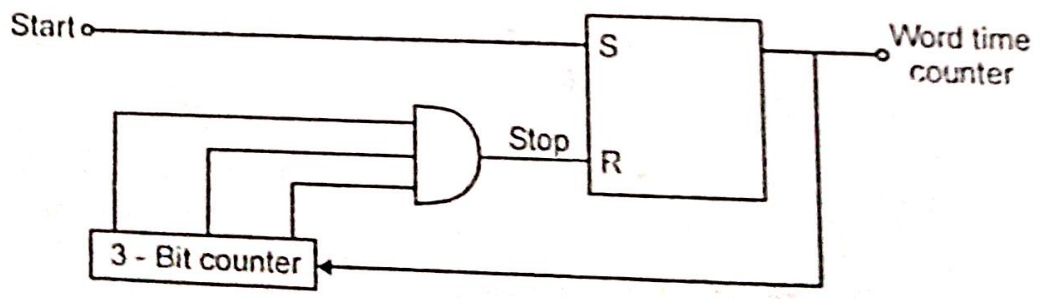


Figure 6.32

Table 3.17. Truth table for 2 bit Synchronous Counter

CLK	Q_B	Q_A
0	0	0
1	0	1
2	1	0
3	1	1

3.8.2. Modulus-N-Counters

The counter with 'n' flipflops has maximum MOD number 2^n. Find the number of flipflops (n) required for the desired MOD number (N) using the equation.

$$2^n \geq N$$

(i) For example, a 3 bit binary counter is a MOD 8 counter. The basic counter can be modified to produce MOD numbers less than 2^n by allowing the counter to skin those are normally part of counting sequence.

$$n = 3$$

$$N = 8$$

$$2^n = 2^3 = 8 = N$$

(ii) MOD 5 Counter:

$$2^n = N$$

$$2^n = 5$$

$2^2 = 4$ less than N

$2^3 = 8 > N\ (5)$

$\therefore$ 3 flipflops are required.

(iii) MOD 10 Counter:

$$2^n = N = 10$$

$2^3 = 8$, less than N ;

$2^4 = 16 > N\ (10)$

$\therefore$ 4 flipflops required.

To construct any MOD-N counter, the following method can be used.

1. Find the number of flipflops (n) required for the desired MOD number (N) using the equation, $2^n \geq N$.
2. Connect all the flipflop as a required counter.
3. Find the binary number for N.
4. Connect all flipflop outputs for which $Q = 1$ when the count is N, as inputs to NAND gate.
5. Connect the NAND gate output to the CLR input of each flipflop.

When the counter reaches N^{th} state, NAND gate goes LOW, resulting all flipflops to 0. Therefore, the counter counts from 0 through $(N-1)$.

For example, MOD-10 counter reaches state 10 (1010). i.e., $Q_3Q_2Q_1Q_0 = (1010)$. The output Q_3 and Q_1 are connected to the NAND gate and the output of NAND gate goes LOW and resetting all flipflops to zero. Therefore MOD-10 counted counts from 0000 to 1001 and then recycles to the zero value. The MOD-10 counter circuit is shown in Fig. 3.51.

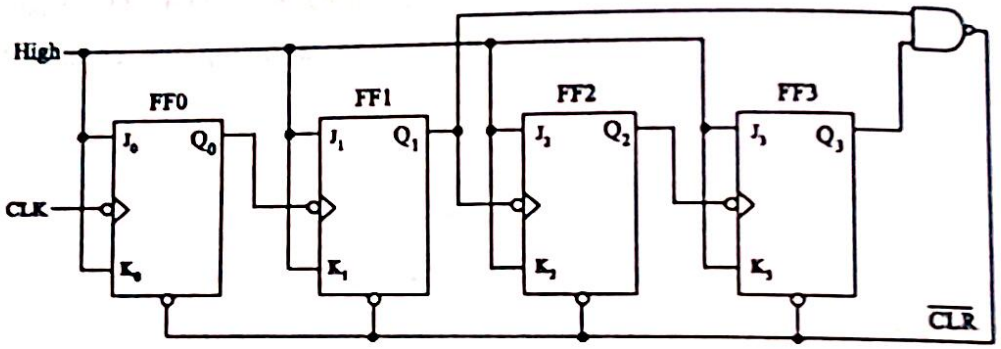


Fig. 3.51. MOD-10 (Decade) Counter

3.8.3. Shift Register Counters

A shifter counter is a basically a shift register with the serial output connected back to the serial input to produce special sequences. Two of the most common types of shift register counters are:

(i) Johnson Counter (Shift Counter).

(ii) Ring Counter.

1. Johnson Counter (Shift Counter)

In a Johnson counter, the complement of the output of the last flip-flop is connected back to the D input of the first flip-flop. This feedback arrangement produces a characteristic sequence of states as shown in Table 3.18. for a 4 bit Johnson counter. The 4 bit sequence has a total of eight states. In general, a Johnson counter will produces a modulus of $2n$, where 'n' is the number of stages in the counter. For example 5 bit Johnson counter has 10 states.

The timing diagram for the left and right shift register resembles the preceding ones. If it is a 4-bit shift register, it requires 4 clock pulses to shift a bit of bit of data to the serial output. After 4 clock pulses, the parallel output will contain the data. If a serial output is required, 3 more clock pulses are necessary. Hence to shift a 4-bit data to the serial output 2n-1 pulses are required.

6.9 Analog to Digital Converters

Analog to digital converters is a digital network which converts analog signal into digital signal. The basic block diagram of Analog to digital converter is shown in figure 6.42.

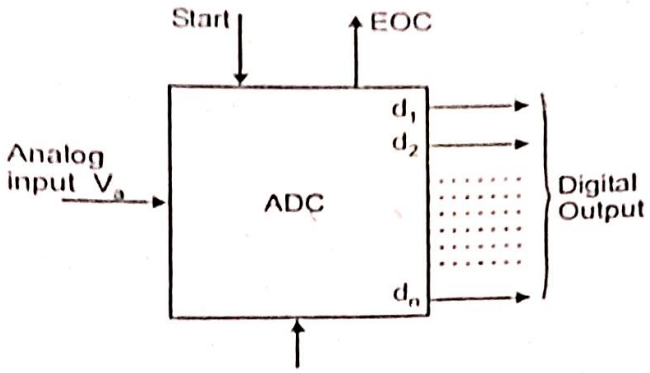


Figure 6.42

When analog input is given, an output binary data of $d_1, d_2, ... d_n$ is produced as function of D.

$$D = d_1 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n}$$

Analog to digital converter has two additional control signals. One is START and another one is EOC. START informs the converter when to start the conversion whereas EOC informs when the conversion is complete. EOC stands for 'End of conversion'.

Analog to digital converters are classified as two groups.

1. Direct type
2. Indirect type

Direct type are classified as

1. Flash (comparator) type converter.
2. Staircase type converter.
3. Tracking or servo converter.
4. Successive approximation type converter.

Indirect type are classified as

1. Charge balancing analog to digital converter.
2. Dual slope analog to digital converter.

Successive Approximation Method

Figure 6.43 shows an 8-bit converter which requires 8 clock pulses to obtain digital output. It consists of successive approximation register (SAR), operational amplifier, and D/A converter. SAR is used to find the required value of each bit by trial and error.

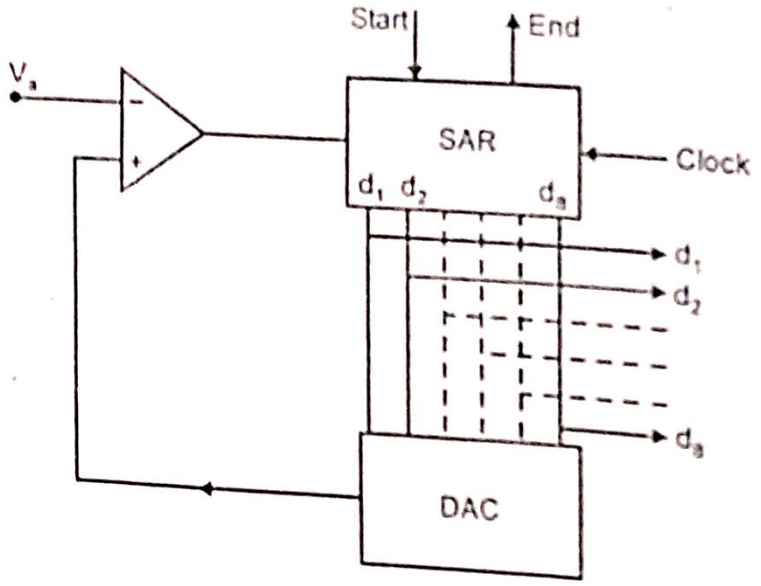


Figure 6.43

When START command is given, SAR sets MSB, $d_1 = 1$ with all other bits to zero so that the trial code is 1000 0000. The output V_d from DAC is now compared with analog input V_a. If $V_a > V_d$, then 1000 0000 is less than correct digital representation.

The MSB will remains at '1' and next bit is made '1' and further tested. But, when $V_a < V_d$ it indicates that 1000 0000 is greater than correct digital representation. Now MSB reset to '0' and go on to the next lower significant bit.

This procedure is repeated for all subsequent bits (i.e., from MSB to LSB), one at a time, until all bit positions have been tested. When DAC output crosses V_a, the comparator changes the state and this is taken as end of conversion (EOC) command. Now, the data available on SAR will be the digital equivalent of the given analog signal.

Advantages

1. High resolution
2. It is very versatile
3. High speed

The Staircase Ramp Type

Figure 6.44 shows basic block diagram of a stair case ramp type analog to digital converter. It consists of comparator DAC, AND gate, counter and display unit.

The basic principle is that the input signal V_a is compared with an internal stair case voltage V_c, generated by a series circuit consisting of a pulse generator (clock), a counter counting the pulses and a digital to analog converter, converting the counter output into a dc signal.

As soon as V_c is equal to V_a, the input comparator closes a gate between the clock and counter, the counter stops and its output is shown on the display.

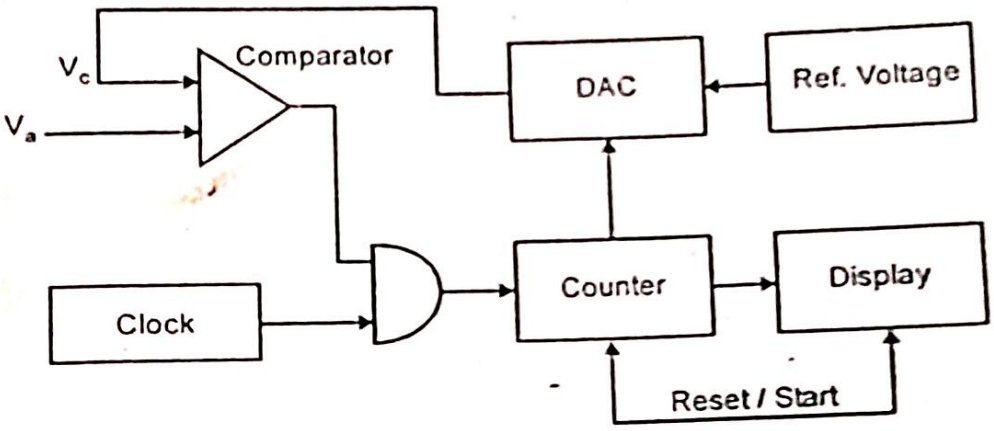


Figure 6.44

Operation

The clock generates pulses continuously. At the start of a measurement, the counter is reset at 0 at time t_1 so that the output of the digital to analog converter is also zero.

If V_a is not equal to zero, the input comparator applies an output voltage that opens the gate so that clock pulses are passed on to the counter through gate. The counter starts counting and the DAC starts to produce an output voltage increasing by one small step at each count of the counter. The result is a stair case voltage applied to the second input of the comparator, as shown in figure 6.45.

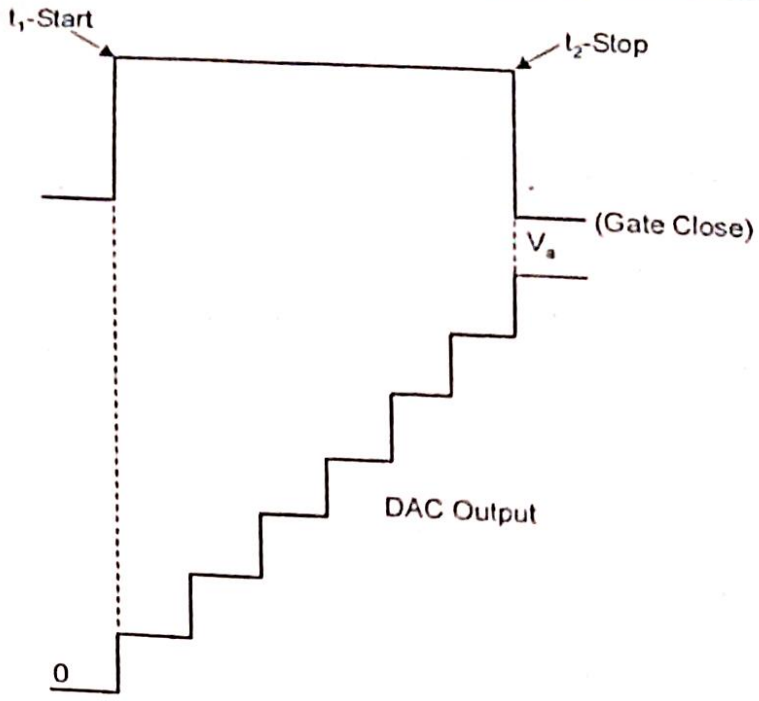


Figure 6.45

This process continues until the staircase voltage is equal to or slightly greater than the input voltage V_a. At instant t_2, the output voltage of the input comparator changes state or polarity, so that the gate closes and counter is stopped. The display unit shows the result of the count.

6.10 Digital to Analog Converters

Digital to analog converters are those which is used to convert digital signals into analog signals. The role of digital to analog converters in instrumentation systems are that, in some applications it is required to convert digital signal into analog signal before processing like computer driver CRT display and digital control of automatic process control systems etc.

Basic Block Diagram

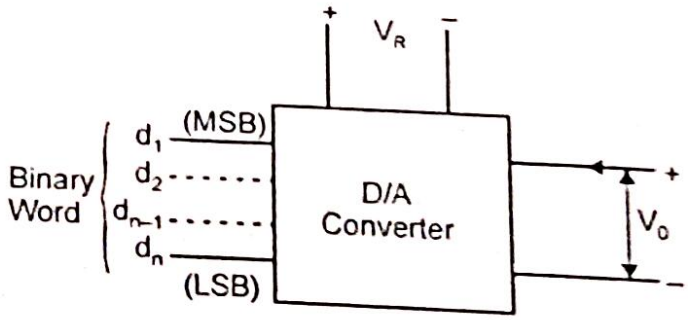


Figure 6.46

Figure 6.46 shows basic block diagram of digital to analog converter. The input is n-bit binary word and is combined with reference voltage to give an analog output signal. The output of digital to analog converter is either a voltage or current. The output voltage of n-bit digital to analog converter is given by

$$V_o = V_R\left(d_1 2^{-1} + d_2 2^{-2} + ... + d_n 2^{-n}\right)$$

where V_R– Reference voltage

$d_1, d_2, \ldots d_n$– n-bit binary words

d_1 – MSB with weight of $V_R/2$

d_2 – LSB with weight of $V_R/2^n$

The different types of digital to analog converters are

1. Binary weighted resistors DAC
2. R-2R ladder
3. Inverted R-2R ladder.

Here, we discussed about binary weighted resistors DAC and R-2R ladder DAC.

Binary Weighted Resistor DAC

The binary weighted resistor DAC uses operational amplifier to sum n binary weighted currents derived from a reference voltage V_R via current scaling resistors 2R, 4R, 8R ... 2^nR. It is shown in figure 6.47.

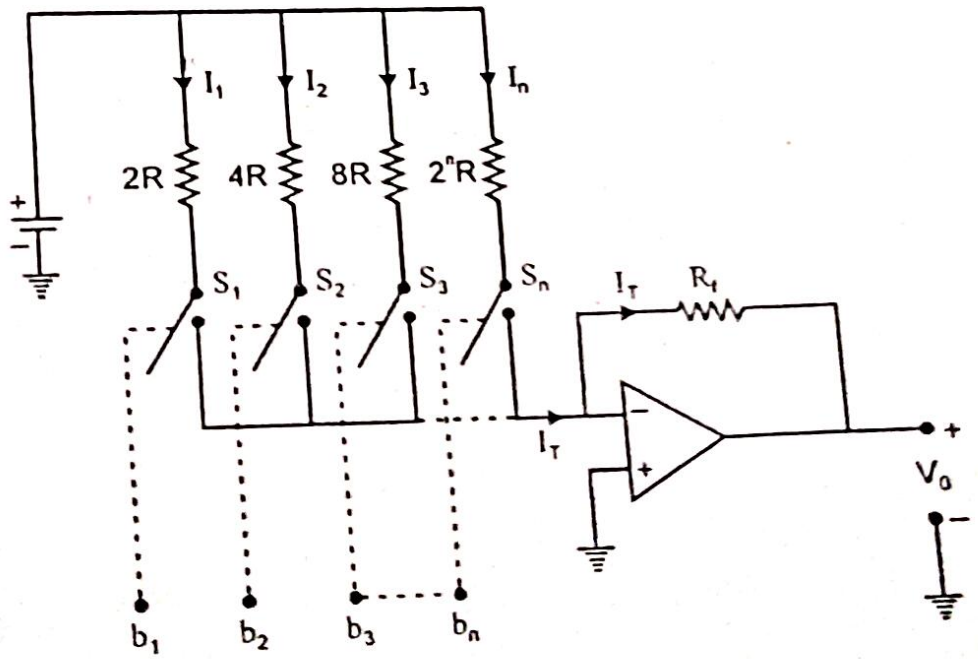


Figure 6.47

Here, the switch positions are controlled by the digital inputs. When the digital input is one, the corresponding switch is closed and digital input is zero, the switch is opened.

Here, the operational amplifier is used as a summing amplifier. Due to the high input impedance of op-amp, summing current will flow through feedback resistor R_f. Now, the total current is

$$I_T = I_1 + I_2 + I_3 + ... + I_n$$

The output voltage is the voltage drop across R_f and it is given as

$$V_0 = -I_T R_f$$

$$= -(I_1 + I_2 + I_3 + ... + I_n) R_f$$

$$= -\left(d_1 \frac{V_R}{2R} + d_2 \frac{V_R}{4R} + d_3 \frac{V_R}{8R} + ... + d_n \frac{V_R}{2^n R}\right) R_f$$

$$= -\frac{V_R}{R}\left(d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + ... + d_n 2^{-n}\right)$$

when $R_f = R$, the output voltage becomes

$$\boxed{V_0 = -V_R\left(d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + ... + d_n 2^{-n}\right)}$$

From this equation, analog output voltage is directly proportional to the input digital data.

R-2R Ladder

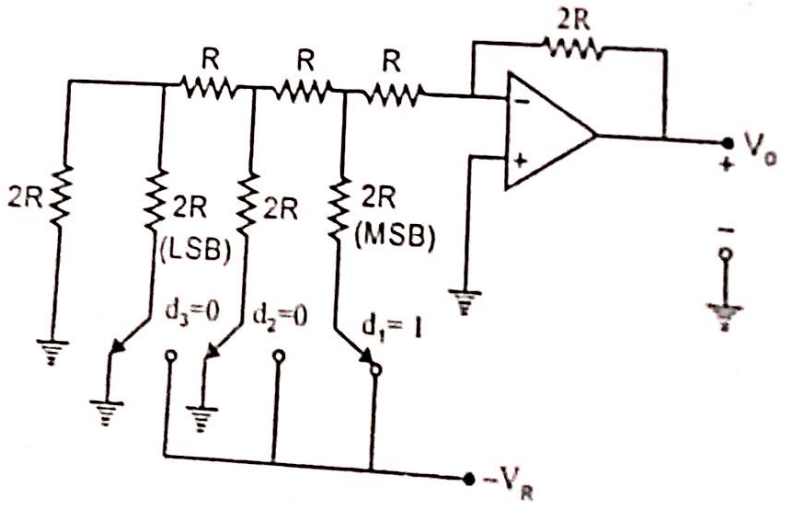


Figure 6.48

Figure 6.48 shows R-2R ladder network. The input to the ladder network must switch from a voltage representing '1' to ground representing '0'. It should be never be left open circuited. The resistors which is load, is same for all bits of digital input. Figure 6.48 shows 3-bit DAC.

The switch positions d_1, d_2, d_3 corresponds to the binary word '100'. The circuit can be simplified to the equivalent form. It is shown in figure 6.49.

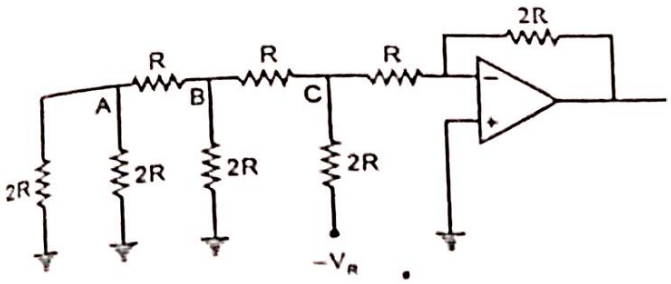


Figure 6.49

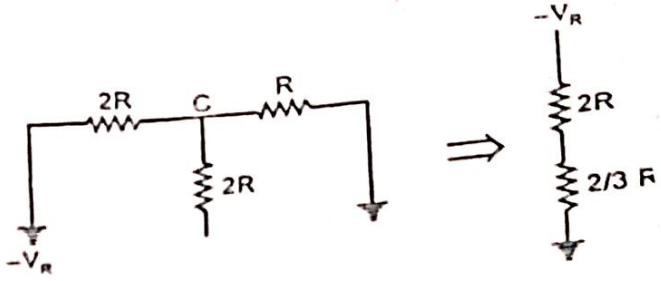


Figure 6.50

From figure 6.49, the equivalent resistance at node 'A' with respect to ground is R.

$$2R \| 2R = \frac{2R \times 2R}{2R + 2R} = R$$

The resistance between node 'B' and ground = R + R = 2R.

Now, the equivalent resistance at node 'B' = $2R \| 2R = R$

The resistance between node 'C' and ground = R + R = 2R as shown in figure 6.49.

Now from figure 6.50, the equivalent resistance at node 'C' with respect to ground.

$$= \frac{2R \times R}{2R + R} = \frac{2}{3}R$$

From figure 6.50, the voltage at node 'C' is calculated as

$$\frac{-V_R\left(\frac{2R}{3}\right)}{2R + \frac{2R}{3}} = \frac{\frac{-2}{3}V_R R}{\frac{8R}{3}} = \frac{-V_R}{4}$$

Then, output voltage $V_0 = \frac{-2R}{R}\left(\frac{-V_R}{4}\right)$

$$\boxed{V_0 = \frac{V_R}{2}}$$

The output voltage of digital to analog converter is proportional to the sum of the weights represented by the switches.

Advantages

1. High resolution
2. High accuracy
3. It requires only two values of resistors, R and 2R, regardless of number of bits digital input.

Two Mark Questions and Answers

1. Define the terms BIT and BYTE.

BIT: It is an abreviation of the words binary digit and smallest unit of information. It is either '0' or '1'.

BYTE: It is a string or gorup of eight bits.

2. Explain the radix of a number system.

Radix or base of a number system is defined as the number of different symbols used in the number system. For example binary number system uses two different symbols '0' and '1'. Thus it has a radix of 2.

3. What is decimal system of number representation?

The decimal number system has ten different symbols or digits i.e., 0, 1, 2, 3, 4, 5, 6, 7, 8 and 9. All higher numbers in this system are represented in terms of these ten digit only. The decimal system has a radix of 10. It is a positional system i.e., each digit in a given decimal number has a weight or a value.

4. Explain the octal and hexadecimal number systems.

Octal number system

It has eight basic symbols. They are 0, 1, 2, 3, 4, 5, 6 and 7. The next digit after 7 in this system will be 10 following by 11, 12, 13 and so on. The octal has a radix or base of 8. Each digit in the octal number system has a place value or weight.

Hexadecimal number system

It has sixteen basic digits or symbols. They are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F. After reaching F, two digit combinations are formed taking the second digit followed by the first digit and so on. The hexadecimal system has a radix or base of 16. Each digit in the hexadecimal number has a place value or weight.