INTRODUCTION

The field-effect transistor (FET) is a three terminal semiconductor device in which the output current is controlled by an applied electric field. Further the current in a FET is entirely due to the majority carriers whereas in a junction transistor both majority and minority carriers contribute to current. Thus, while the junction transistor is bipolar, a FET is unipolar. There are two types of field-effect transistors : (*i*) *junction field effect transistor* (JFET or simply FET). (*ii*) *metal oxide semiconductor field effect transistor* (MOSFET). A JFET can be either of the *n*-channel type or of *p*-channel type. We shall here describe an *n*-channel JFET.

***n*-channel JFET.** It consists of a channel (*n*-type) into which two *p*-regions are diffused. One end of this symmetric structure is called *source* (*S*) and the other end is called *drain* (*D*). The two *p*-regions are connected together to a third terminal called *gate* (*G*) (Fig. 38.1). The *p*-regions are heavily doped compared to the *n*-region. During operation, majority carriers (electrons in this case) enter the channel through the source *S* and leave it through the drain *D*. The current is controlled by the gate which is always *reverse-biased.*

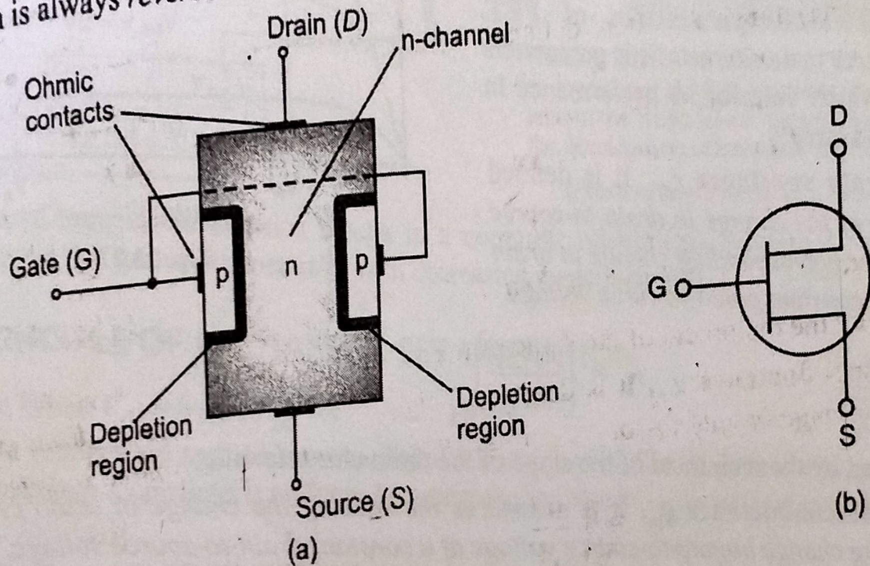


Fig. 38.1

38.2 DRAIN CHARACTERISTICS OF AN N-CHANNEL JFET

A curve plotted between drain current i_D and drain-to-source voltage V_{DS}, at a fixed gate-to-source voltage V_{GS} is called the drain characteristics. Fig. 38.2 shows the circuit diagram for determining the output characteristics. V_{GG} is the gate bias supply and V_{DD} is the drain voltage source.

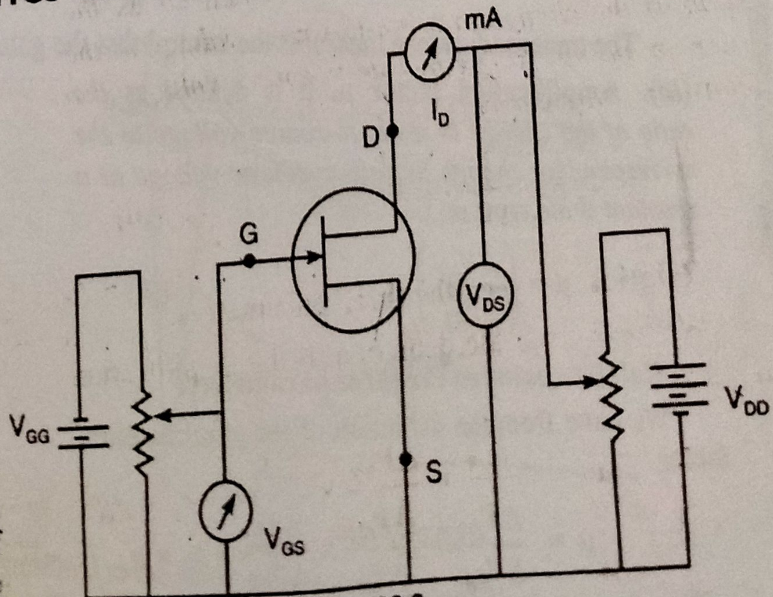


Fig. 38.2

Keeping V_{GS} fixed at some value, the drain source voltage (V_{DS}) is changed in steps and the corresponding drain current I_D is noted. A group of such drain characteristics curves are drawn by setting V_{GS} at different fixed

values. Fig. 38.3 shows a family of drain characteristics. There are three distinct regions in the characteristic thus obtained.

(*i*) When V_{DS} is small, the channel acts as a resistor. The current increases linearly with the voltage V_{DS} till point *A* is reached. This region of the characteristic is called the *ohmic region.*

(*ii*) When $V_{DS} = V_P$, the current I_D reaches its maximum value, I_{DSS}. If V_{DS} is increased beyond V_P, the current does not increase any further. The region *BC* is called saturation region or *pinch off region.*

(*iii*) *At a certain voltage* V_A, corresponding to point *C*, current increases suddenly due to avalanche breakdown. The covalent bonds in the depletion region break up and the current rises. This region is called the *avalanche region.* In actual practice this region is to be avoided.

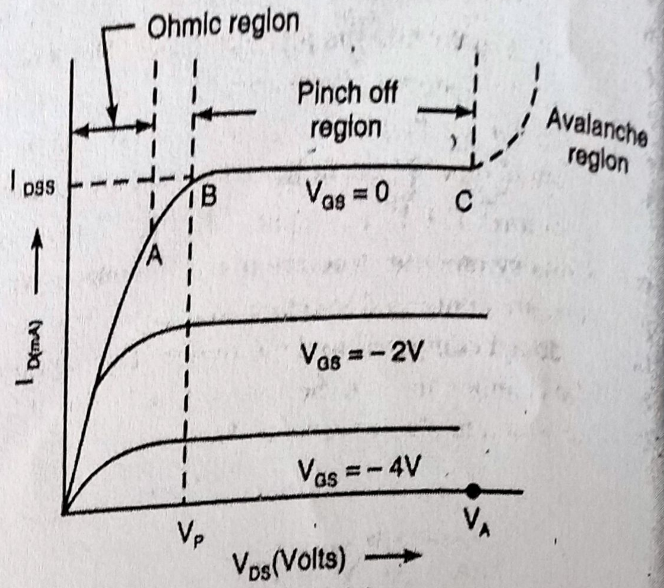


Fig. 38.3

Characteristic parameters of FET. There are three main characteristic parameters of a FET which describe its performance in an electronic circuit.

(*i*) **Drain resistance r_d.** It is defined as *the ratio of the change in drain-to-source voltage to the corresponding change in drain current at a constant gate-to-source voltage.*

$$r_d = \left(\frac{\Delta V_{DS}}{\Delta I_D}\right)_{V_{GS}} \quad ...(i)$$

It is given by the reciprocal of the slope of the drain characteristic.

(*ii*) **Transconductance g_m.** It is defined as *the ratio of the change in drain current to the corresponding change in gate-to-source voltage at a constant drain-to-source voltage.*

$$g_m = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right)_{V_{DS}} \quad ...(ii)$$

The transconductance measures the control that the gate voltage has over the drain current.

(*iii*) **Amplification factor μ.** It is defined as *the ratio of the change in drain-to-source voltage to the corresponding change in gate-to-source voltage at a constant drain current.*

$$\mu = \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_D} \quad ...(iii)$$

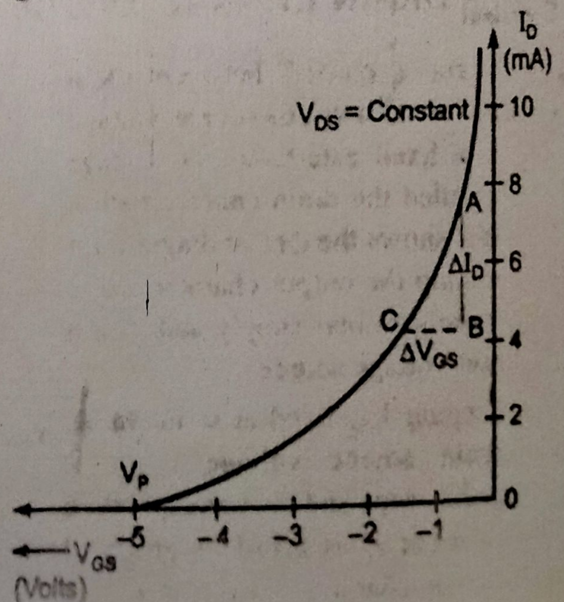


Fig. 38.4

Relation between the three parameters.

We have from the definition of the amplification factor

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = r_d \times g_m$$

$$\mu = r_d \times g_m.$$

(ii) **Transfer characteristics**

The graph drawn between drain current I_D and gate to source voltage V_{GS}, at constant V_{DS} is known as *Transfer characteristics* (Fig. 38.4).

For a constant value of V_{DS}, I_D is noted by varying V_{GS}. The value of V_{GS} (−ve) is varied till I_D becomes zero. This particular voltage V_P where $I_D = 0$ is called *pinch-off voltage*. The slope of the straight line portion of the graph gives the *transconductance* g_m.

$$\text{Transconductance} \quad g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}}$$

William Bradford Shockley (1910-1989), co-inventor of the first transistor and formulator of the "field-effect" theory employed in the development of transistor and the FET.

(Photo courtesy of AT & T Archives.)

The transconductance is determined from the transfer characteristic curve.

$$g_m = \frac{AB}{BC} = \text{Slope of the curve.}$$

The relationship between I_D and V_{GS} is defined by *Shockley's equation.*

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Control variable (V_{GS}); Constants (I_{DSS}, V_P)

The squared term in the equation results in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitude of V_{GS}.

38.3 PRINCIPLE OF N-CHANNEL FET OPERATION

Case (i): When $V_{GS} = 0$ and $V_{DS} = 0$

When no voltages are applied between D and S and G and S, the thickness of the depletion regions around the p-n junctions is uniform. So a rectangular channel with uniform cross-section is formed [Fig. 38.1 (a)].

Case (ii): $V_{GS} = 0$ V, V_{DS} Some Positive Value

A positive voltage V_{DS} is applied across the channel and the gate is connected directly to the source to establish the condition $V_{GS} = 0$ V [Fig. 38.5 (a)].

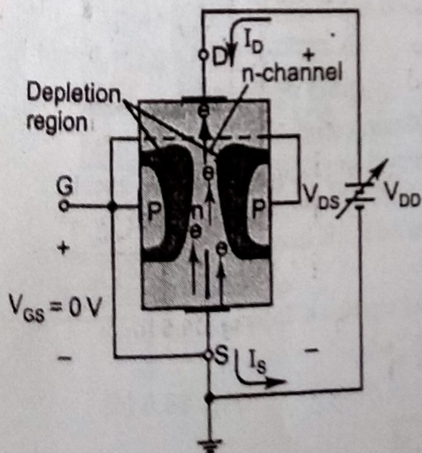


Fig. 38.5 (a)

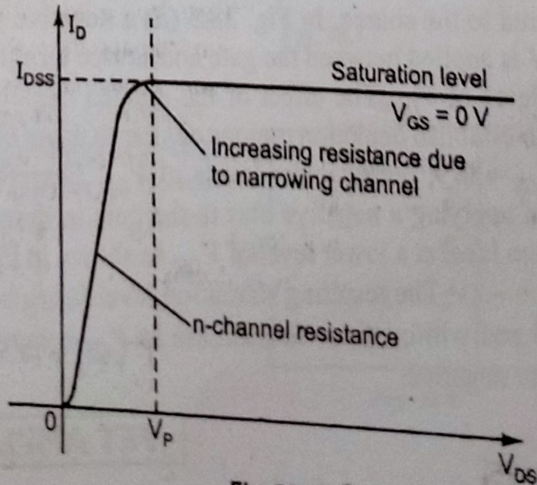


Fig. 38.5 (b)

The result is a gate and a source terminal at the same potential and a depletion region in the low end of each p-material similar to the distribution of the no-bias conditions of Fig. 38.1 (a). The

instant the voltage V_{DD} ($= V_{DS}$) is applied, the electrons are drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 38.5 (*a*). The path of charge flow reveals that the drain and source currents are equivalent ($I_D = I_S$). The flow of charge is relatively uninhibited and is limited solely by the resistance of the n-channel between drain and source. The depletion region is wider near the top of both p-type materials.

- As the voltage V_{DS} is increased from 0 V to a few volts, the current will increase as determined by Ohm's law. The plot of I_D versus V_{DS} will appear as shown in Fig. 38.5 (*b*). The relative straightness of the plot reveals that for the region of low values of V_{DS}, the resistance is essentially constant. As V_{DS} increases and approaches a level referred to as V_P, the depletion regions will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region. If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" as shown in Fig. 38.5 (*c*), a condition referred to as *pinch-off* will result. The level of V_{DS} that establishes this condition is referred to as the *pinch-off voltage* and is denoted by V_P.

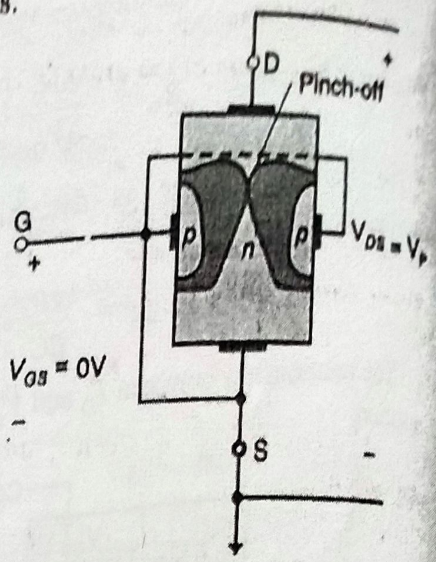


Fig. 38.5 (c)
Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

- As V_{DS} is increased beyond V_P, the region of close encounter between the two depletion regions increases in length along the channel, but the level of I_D remains essentially the same.
- *I_{DSS} is the maximum drain current for a JFET and is defined by the conditions*

$$V_{GS} = 0\text{ V} \quad \text{and} \quad V_{DS} > |V_P|.$$

Case (*iii*): $V_{GS} < 0$ V

The controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source. In Fig. 38.5 (*d*) a negative voltage of -2V is applied between the gate and source terminals for a low level of V_{DS}. The effect of the applied negative-bias V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V, but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS}, as shown in Fig. 38.3 for $V_{GS} = -2$V. The resulting saturation level for I_D has been reduced and will continue to decrease as V_{GS} is made more and more negative.

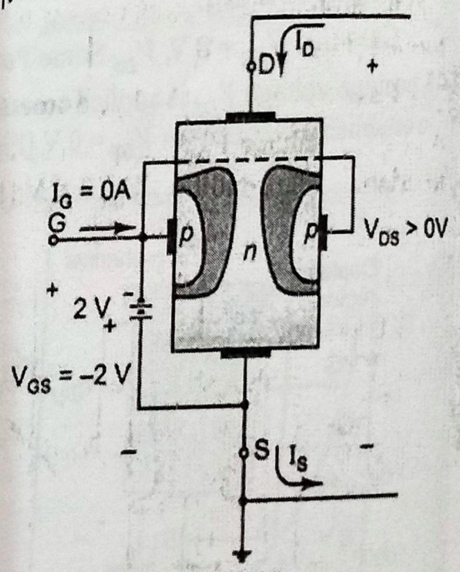


Fig. 38.5 (d)

FET AMPLIFIER

38.4 COMMON SOURCE FET AMPLIFIER

Fig. 38.6 shows the common source amplifier circuit. V_{GG} is the gate bias battery. The ac signal to be amplified is applied between the gate and the source. The load resistance R_L is connected

...ween the supply battery V_{DD} and the drain D. The ...put is taken across the load R_L or across the FET. ...the output ac voltage be v_{ds} for an input signal ...tage v_{gs}.

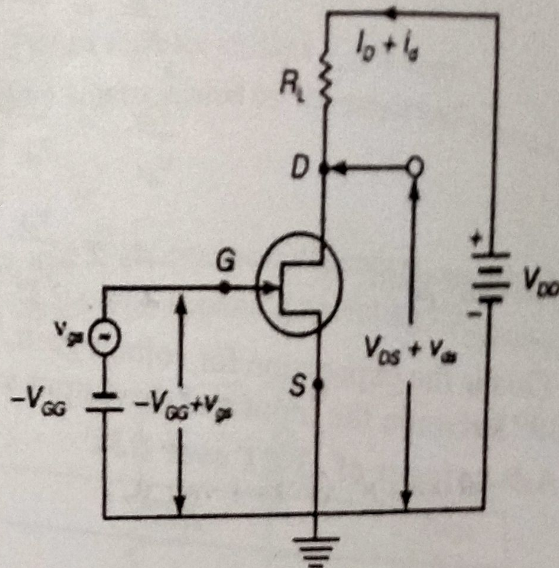


Fig. 38.6

Working. On applying an alternating signal, ...fixed reverse bias of the gate changes. A small ...nge in the reverse bias gate voltage, produces a ...ge change in drain current. This fact makes FET ...pable of amplifying weak signal. The amplifying ...tion of FET can be explained using its transfer characteristics (Fig. 38.7).

When the signal (v_{gs}) is not applied, the gate to source voltage is given by OA. The corresponding drain current is given by OF. When the signal is applied, during the positive half cycle of the input signal ($+v_{gs}$), the reverse bias on the gate decreases ($-V_{GG} + v_{gs}$). The gate to source voltage decreases from OA to OC. Due to this, the channel width increases. Hence, drain current increases from OF to OG. During the negative half of the signal ($-v_{gs}$), the reverse voltage on the gate increases ($-V_{GG} - v_{gs}$) to OB. Due to this the channel width decreases. Hence the drain current decreases to OE. Thus, a small change in the gate to source voltage, produces a large change in drain current and hence large change in output voltage. Thus, FET works as an amplifier.

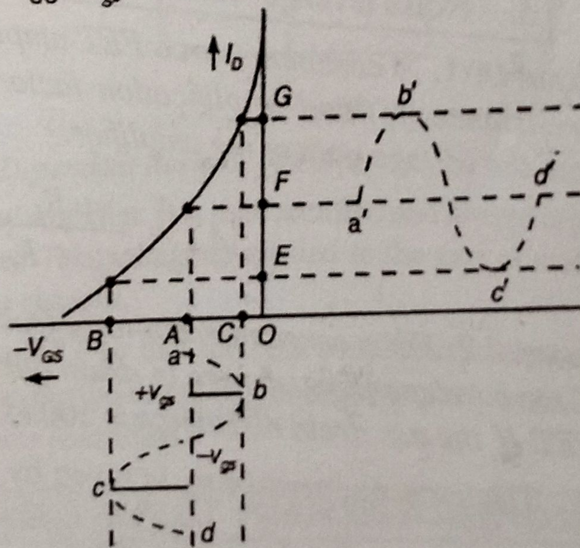


Fig. 38.7

When the signal voltage is positive, the gate becomes less negative with respect to the source. The drain current is enhanced, causing a large voltage drop across R_L which makes the drain terminal less positive with respect to the source. Since an increase of the gate voltage causes a decrease in the drain voltage, there is a phase shift of 180° between the input and output of the FET amplifier.

Expression for Voltage Gain

The a.c. voltage source equivalent circuit of FET amplifier is shown in Fig. 38.8. FET can be replaced by a voltage generator $-\mu v_{gs}$ in series with drain resistance r_{ds}. i_d is the ac current flowing through the load R_L. The output ac voltage is v_{ds} for an input signal voltage v_{gs}.

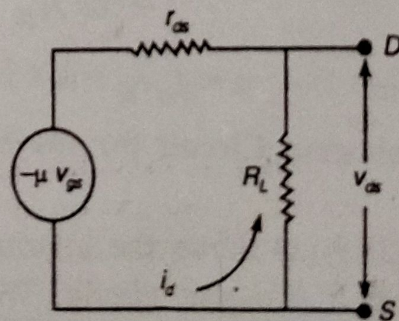


Fig. 38.8

Applying Kirchoff's voltage law to the circuit,

$$-\mu v_{gs} = i_d R_L + i_d r_{ds}$$

$$\therefore \quad i_d = \frac{-\mu v_{gs}}{r_{ds} + R_L}$$

$$v_{ds} = i_d . R_L$$

But

$$i_d = \frac{v_{ds}}{R_L}$$

$$\therefore \quad \frac{v_{ds}}{R_L} = \frac{-\mu v_{gs}}{r_{ds} + R_L}$$

$$\frac{v_{ds}}{v_{gs}} = \frac{-\mu R_L}{r_{ds} + R_L}$$

Voltage gain $\quad A_v = \frac{v_{ds}}{v_{gs}} = \frac{-\mu R_L}{r_{ds} + R_L}$

This is the expression for voltage gain. The negative sign indicates that there is a phase difference of 180° between the input and the output voltages.

Advantages of JFET over BJT

	BJT	*FET*
1.	Bipolar	Unipolar
2.	Input impedance low	Input impedance high
3.	Current controlled	Voltage controlled
4.	Characterised by current gain	Characterised by transconductance
5.	Noise level not small	Noise level very small

EXAMPLE 1. *A common-source FET amplifier has a load resistance R_L = 500 kΩ. If the a.c. drain resistance (r_d) and amplification factor (μ) of the FET are 100 kΩ and 24, respectively, calculate the voltage gain of the amplifier.*

SOL.

$$|A_v| = \frac{\mu R_L}{r_{ds} + R_L} = \frac{24 \times 500 \times 10^3}{100 \times 10^3 + 500 \times 10^3} = 20.$$

EXAMPLE 2. *For a constant drain-to-source voltage if the gate-source voltage is changed from 0 to –2 V, the corresponding change in drain current becomes 2 mA. Calculate the transconductance of the FET. If the a.c. drain resistance is 100 kΩ, calculate also the amplification factor of the FET.*

SOL. The transconductance g_m is given by

$$g_m = \left(\frac{\Delta I_D}{\Delta V_{GS}}\right)_{V_{DS}} = \frac{2\,mA}{2V} = 1\,\text{mA/V}.$$

Again, $\quad \mu = g_m r_{ds} = 1 \times 10^{-3} \times 100 \times 10^3 = 100.$

The Equivalent Circuit for the FET (Low frequency model)

Fig. 38.9 (*a*) shows the internal elements of a FET arranged as a two–port circuit. We can reduce it to a simpler equivalent form as in (*b*) by consideration of the relative magnitudes of the resistances and the reactances.

The input element r_{gs} is the reverse – biased junction resistance of a JFET or the silicon-dioxide insulation resistance of a MOSFET. These resistances exceed 10^8 ohms. We will consider the input of a FET as an open circuit.

(a)

$$g_d = g_{d0}\left[1-\left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]$$

where g_{d0} is the value of drain conductance when the bias voltage V_{GS} is zero.

The variation of the r_d with V_{GS} can be closely approximated by the empirical expression,

$$r_d = \frac{r_0}{1-KV_{GS}}$$

where r_0 = drain resistance at zero gate bias, and K = a constant, dependent upon FET type.

Thus, small signal FET drain resistance r_d varies with applied gate voltage V_{GS} and FET acts like a variable passive resistor.

FET finds wide applications where VVR property is useful. For example, the VVR can be used in *Automatic Gain Control* (AGC) circuit of a multistage amplifier.

The VVR is used to vary the voltage gain of a multistage amplifier. If the signal is low then voltage gain of the stages can be increased and when the signal becomes high, the gain can be reduced automatically. In this way, the general level of amplification is maintained fairly constant.

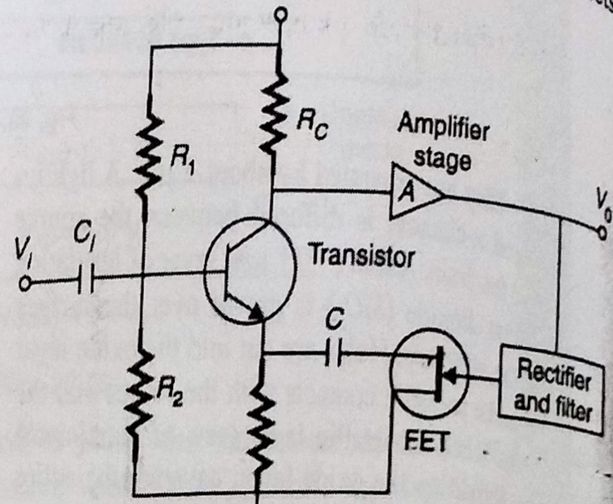


Fig. 38.15

Circuit. Fig. 38.15 shows the circuit arrangement of AGC amplifier using the FET as *Voltage Variable Resistor* (*VVR*) or *Voltage Dependent Resistor* (*VDR*).

Working. The input signal v_i is amplified by amplifier. It is then rectified and filtered to produce a d.c. voltage proportional to output signal level. This voltage is applied to the gate of the FET so that the a.c. resistance between drain and source changes.

The capacitor C isolates the transistor from FET so that the bias conditions of transistor are not affected. So, when output increases, V_{GS} also increases and R_{DS} changes so that the gain of the transistor decreases. Thus automatically the gain is controlled.

METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

There are two types of MOSFETs.

(*i*) The Depletion MOSFET.

(*ii*) The Enhancement MOSFET.

In both types, *p*-channel and *n*-channel versions exist.

38.7 THE DEPLETION MOSFET

Construction

Fig. 38.16 shows the construction of an *n*-channel depletion MOSFET. It consists of a lightly doped *p*-type substrate into which two heavily-doped n^+-regions are diffused. These two n^+ regions act as source *S* and drain *D*.

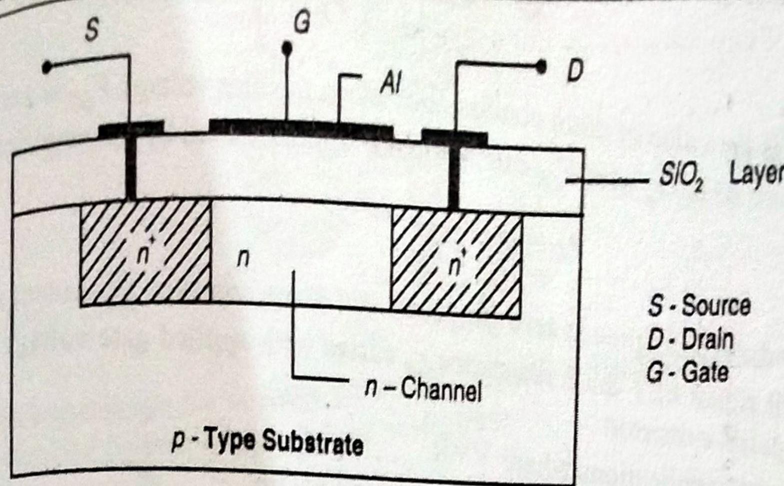


Fig. 38.16

They are separated by about 5 μm. A lightly-doped n-channel is diffused between the source and the drain. A thin (~ 0.1 μm) layer of insulating silicon dioxide (SiO_2) is grown over the surface of the structure. Holes are cut into the oxide layer to make metallic contacts with the source and the drain. Then a metallic layer (say, of aluminium) is overlaid on the oxide layer, covering the entire channel region. This aluminium layer acts as gate (G). Simultaneously, aluminium contacts are made to the source and the drain.

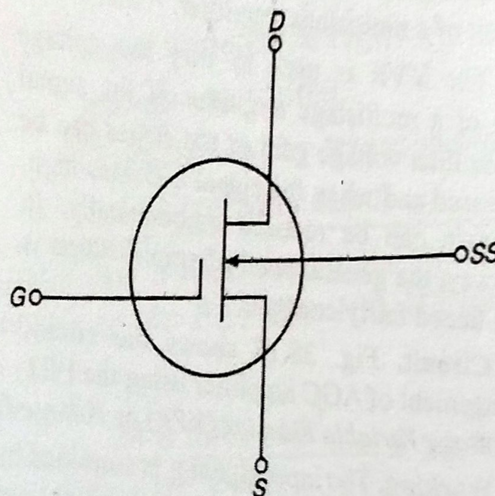


Fig. 38.17

Fig. 38.17 shows the symbol of *n*-channel depletion-type MOSFET. Usually, the substrate terminal *SS* is internally connected to the source terminal *S*.

Operation

Suppose a potential is applied to the gate such that it is positive with respect to source. Then, the positive charge on the gate attracts additional free electrons into the channel from the source. This enhancement of mobile carriers decreases the channel resistance.

Suppose the applied voltage makes the gate negative with respect to source (Fig. 38.18). Then, the negative charge on the gate forces free electrons out of the channel.

A carrier-depletion region is formed on the surface of the silicon at the oxide-silicon interface. The channel is thus constricted by a negative gate voltage. The resistance of the channel increases. When the gate is sufficiently negative, the depletion region extends completely across the channel and joins with depletion region of the *p-n* junction on the other side of the channel. Under this condition, the channel cannot conduct current between drain and source. Thus drain and source become cut off. The negative gate voltage when channel becomes nonconducting is the pinch off voltage V_p.

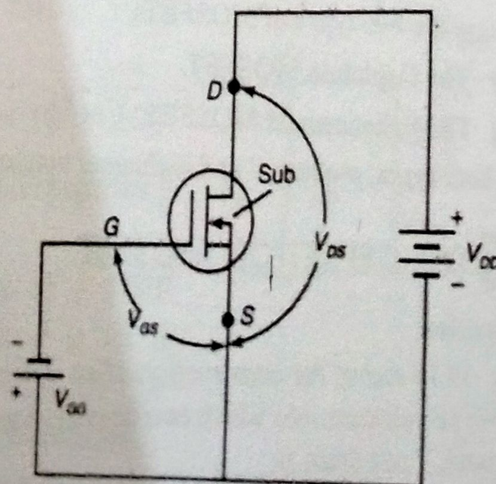


Fig. 38.18

A positive voltage V_{DS} is also applied across the drain *D* and the source *S* (Fig. 38.18). There is a voltage drop along the channel, with the drain end of the channel positive relative to the source end. This further increases the depletion region at the surface.

38.7.1. Static Characteristics of Depletion MOSFET

1. Output or Drain Characteristics. Fig. 38.19 shows the drain characteristic curves (i_D versus V_{DS} at constant V_{GS}) for an n-channel MOSEFT.

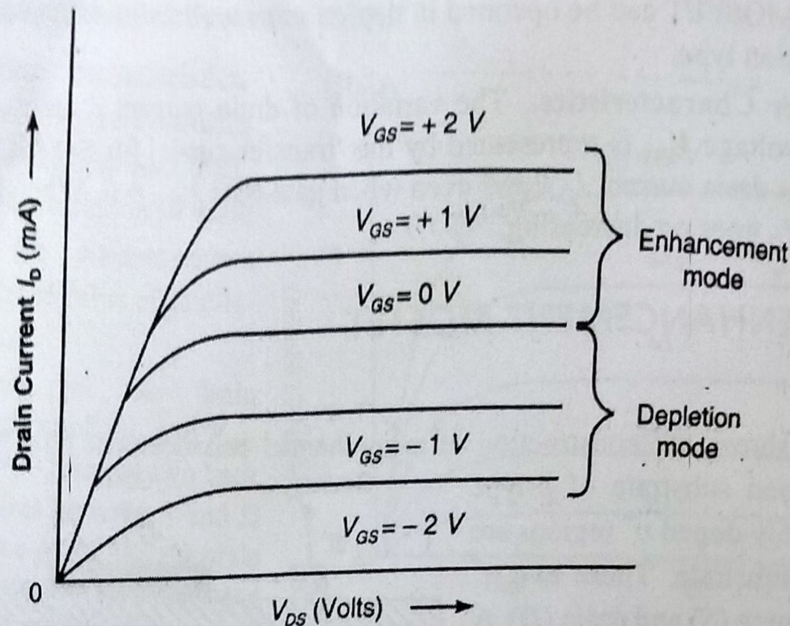


Fig. 38.19

An n-channel MOSFET may be operated in either the enhancement mode or the depletion mode. The enhancement mode occurs for positive values of V_{GS} while the depletion mode occurs for negative values of V_{GS}.

When no gate-to-source voltage is applied ($V_{GS} = 0$), a significant drain current i_D flows due to the flow of majority carriers (electrons) in the n-channel from source to drain under V_{DS}. As V_{DS} increases, i_D increases to a saturation value.

When the gate is made negative, positive charges are induced in the channel through the dielectric SiO_2. This causes depletion of electrons (majority carriers) in the channel. Therefore, the channel becomes less conductive. Consequently, the drain current progressively decreases to almost zero as V_{GS} is made more and more negative, at all values of V_{DS}.

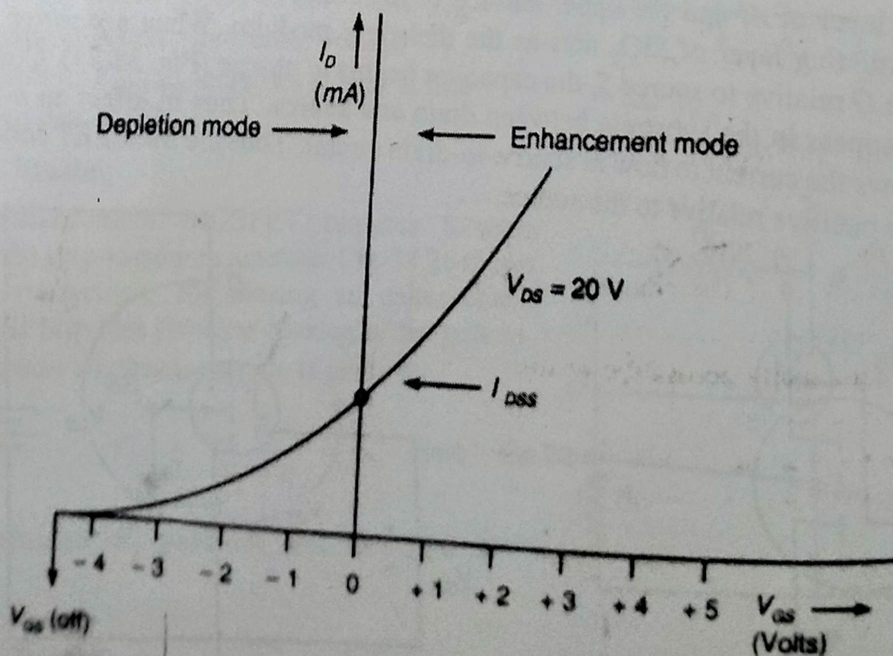


Fig. 38.20

When the gate is made positive, negative charges are induced in the channel, thus enhancing the majority-carriers. Hence the drain current increases above its value at $V_{GS} = 0$, for all V_{DS}.

Thus, this MOSFET can be operated in depletion as well as in enhancement mode although it is termed depletion type.

2. Transfer Characteristics. The variation of drain current I_D with gate voltage V_{GS} at a constant drain voltage V_{DS} is represented by the 'transfer curve' for the MOSFET (Fig. 38.20). It may be seen that drain current I_D flows even when gate-bias $V_{GS} = 0$. When V_{GS} is made more and more negative, I_D goes on decreasing.

38.8 THE ENHANCEMENT MOSFET

Construction

Fig. 38.21 shows the construction of an n-channel enhancement type MOSFET. It consists of a lightly doped substrate of p-type silicon. Two highly doped n^+ regions are diffused in the substrate. These two n^+ regions act as source (S) and drain (D). A thin layer of silicon dioxide (SiO_2) is deposited over the substrate. Then a thin film of metal aluminium is deposited over SiO_2. This aluminium layer acts as gate (G).

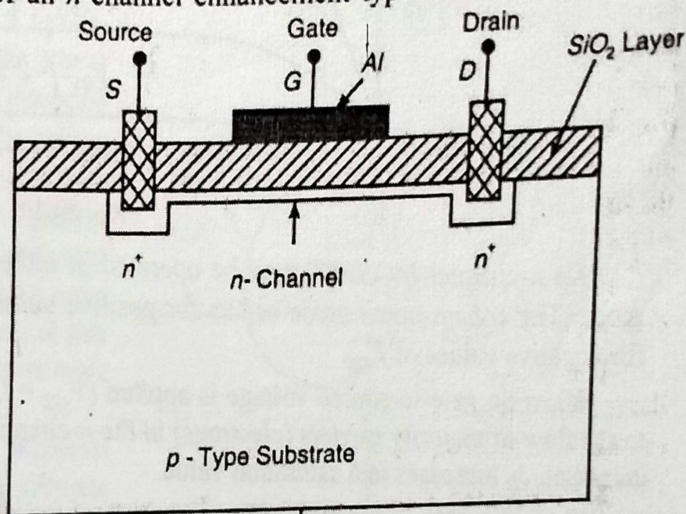


Fig. 38.21

Fig. 38.22 shows the symbol of n-channel E-MOSFET. The vertical line (representing channel) is broken to represent that there is no continuous channel in an enhancement MOSFET.

Operation

The metallic layer of Al and the upper surface of the substrate act as the parallel plates of a capacitor. The insulating layer of SiO_2 acts as the dielectric medium. When a *positive* voltage is applied to the gate G relative to source S, the capacitor begins to charge (Fig. 38.23). Consequently negative charges appear in the substrate between drain and source. Thus in effect an n-channel is created which allows the current to flow in source-to-drain circuit. Thus the MOSFET conducts only when gate is made positive relative to the source.

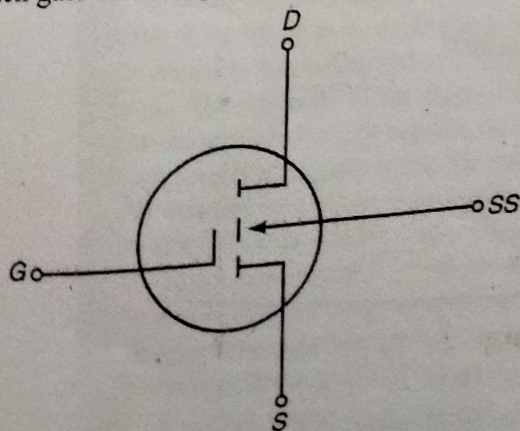


Fig. 38.22

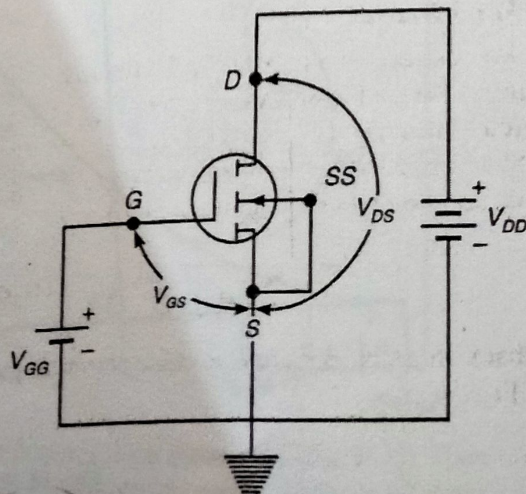


Fig. 38.23

The MOSFET can never operate with a negative gate voltage. The MOSFET is cut-off when $V_{GS} = 0$.

38.8.1. Characteristics of Enhancement MOSFET

1. Output or Drain Characteristics. Fig. 38.24 shows the drain characteristics of an *n*-channel enhancement MOSFET. Each curve shows the variation of drain current I_D with the drain-to-source voltage (V_{DS}) for a fixed value of gate-to-source voltage (V_{GS}).

The magnitude of the drain current I_D is a function of V_{DS} and V_{GS}. When $V_{GS} = 0$, $I_D = 0$ because two back to back *p–n* junctions between *S* and *D* (one between source *S* and the substrate and the other between the substrate and the drain *D*) are reverse biased regardless of the value of V_{DS}.

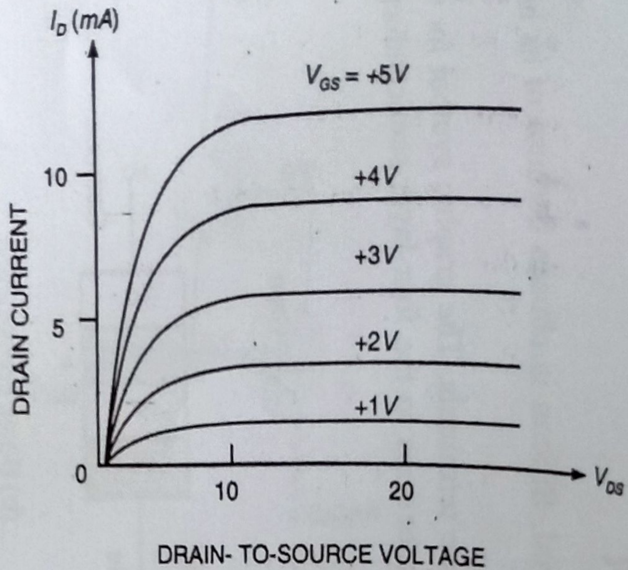


Fig. 38.24

For a fixed positive V_{GS}, the drain current first increases rapidly with V_{DS} and then saturates. It increases for higher values of V_{GS}.

The minimum positive value of V_{GS} at which the drain current is established is called the 'gate-source threshold voltage' V_{GST} or V_T.

2. Transfer Characteristics. The curve showing the variation of drain current I_D with gate-to-source voltage V_{GS} for a fixed value of V_{DS} is called the transfer characteristic. The transfer curve for an *n*-channel enhancement MOSFET is shown in Fig. 38.25. I_D flows only when V_{GS} exceeds gate-to-source threshold voltage V_T. With increase in V_{GS}, I_D increases slowly at first and then rapidly.

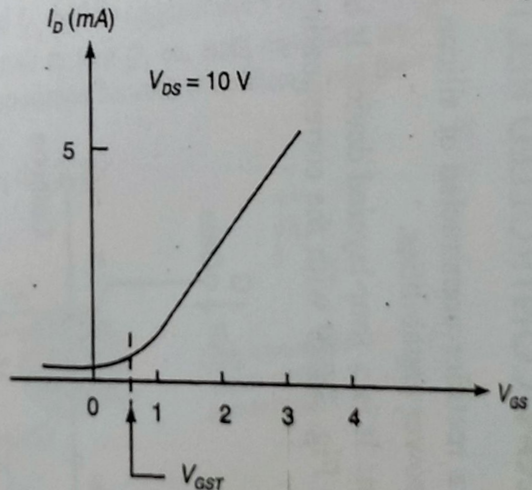


Fig. 38.25

MOSFET Biasing

An enhancement MOSFET requires forward biasing of the gate-to-source junction. Fig. 38.26 shows a circuit arrangement for biasing an enhancement MOSFET. It provides *forward biasing of the gate-to-source junction* whose magnitude is given by

$$V_{GS} = \frac{R_1}{R_1 + R_f} V_{DS}.$$

Here the feedback resistor R_f provides the operating point stability.

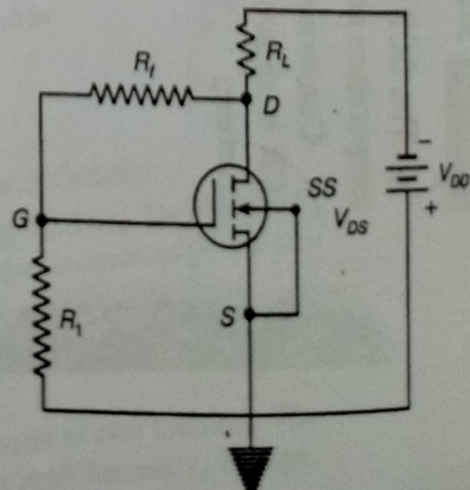


Fig. 38.26

38.10 SILICON-CONTROLLED RECTIFIER

The SCR is a rectifier constructed of silicon material. Silicon is chosen because of its high temperature and power capabilities.

Construction: It is a four-layered device. It has three terminals. The graphic symbol for the SCR is shown in Fig. 38.29 with the corresponding connections to the four-layer semiconductor structure.

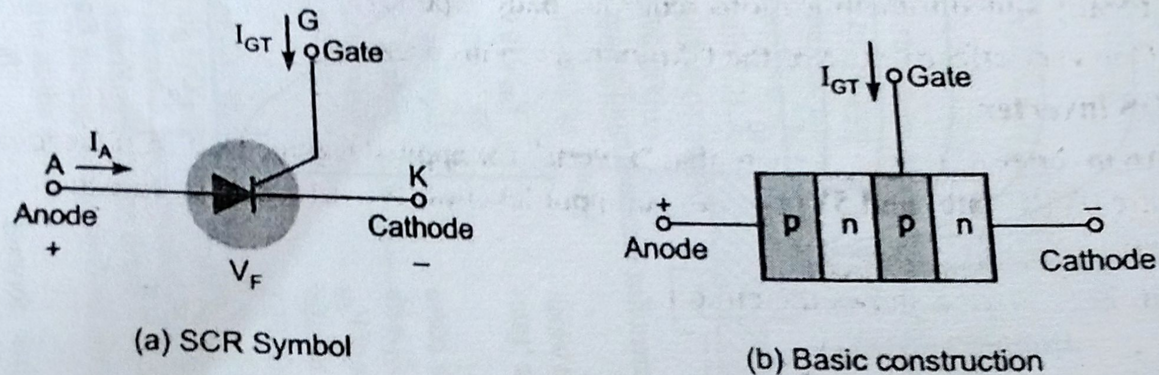


Fig. 38.29

As indicated in Fig. 38.29 *a*, if forward conduction is to be established, the anode must be positive with respect to the cathode. This is not, however, a sufficient criterion for turning the device on. A pulse of sufficient magnitude must also be applied to the gate to establish a turn-on gate current, represented symbolically by I_{GT}.

Basic operation of an *SCR*

The four-layer *pnpn* structure of Fig. 38.29 *b* can be split into two three-layer transistor structures [(Fig. 38.30 (*a*)].

Fig. 38.30 (*b*) shows the *SCR two-transistor equivalent circuit.*

Q_1 is a *pnp* transistor.

Q_2 is an *npn* transistor.

The signal shown in Fig. 38.31 (*a*) is applied to the gate of the circuit of Fig. 38.30 (*b*).

(i) "Off" state of the SCR. **(When Gate is open)**

During the interval $0 \rightarrow t_1$, $V_{gate} = 0$ V, the circuit of Fig. 38.30 (*b*) will appear as shown in Fig. 38.31 (*b*) ($V_{gate} = 0$ V is equivalent to the gate terminal being grounded).

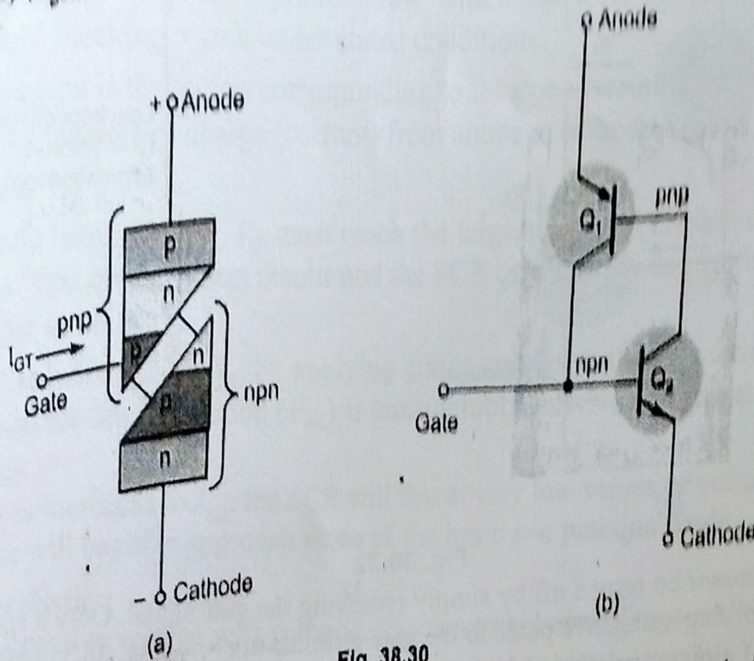


Fig. 38.30

- For $V_{BE_2} = V_{gate} = 0$ V, the base current $I_{B_2} = 0$, and I_{C_2} will be approximately I_{CO}.
- The base current of Q_1, $I_{B_1} = I_{C_2} = I_{CO}$, is too small to turn Q_1 on. Both transistors are therefore in the "off" state, resulting in a high impedance between the collector and the emitter of each transistor.

Fig. 38.31 (*c*) shows open-circuit representation for the SCR.

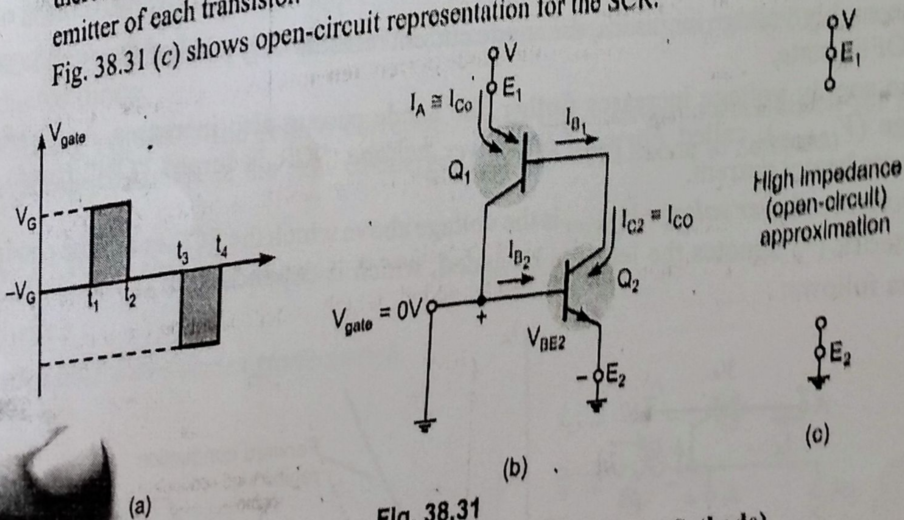


Fig. 38.31

state of the SCR **(When gate is applied +ve voltage w.r.t Cathode)**

At $t = t_1$, a pulse of V_G volts will appear at the SCR gate [(Fig. 38.32 (*a*)]. The potential V_G is chosen sufficiently large to turn Q_2 on ($V_{BE_2} = V_G$). The collector current of Q_2 will then rise to a value sufficiently large to turn Q_1 on ($I_{B_1} = I_{C_2}$).

- As Q_1 turns on, I_{C_1} will increase, resulting in a corresponding increase in I_{B_2}. The increase in base current for Q_2 will result in a further increase in I_{C2}.
- The net result is a regenerative increase in the collector current of each transistor. The resulting anode-to-cathode resistance ($R_{SCR} = V/I_A$) is then small because I_A is large.

Fig. 38.32 (*b*) shows the short-circuit representation for the SCR.

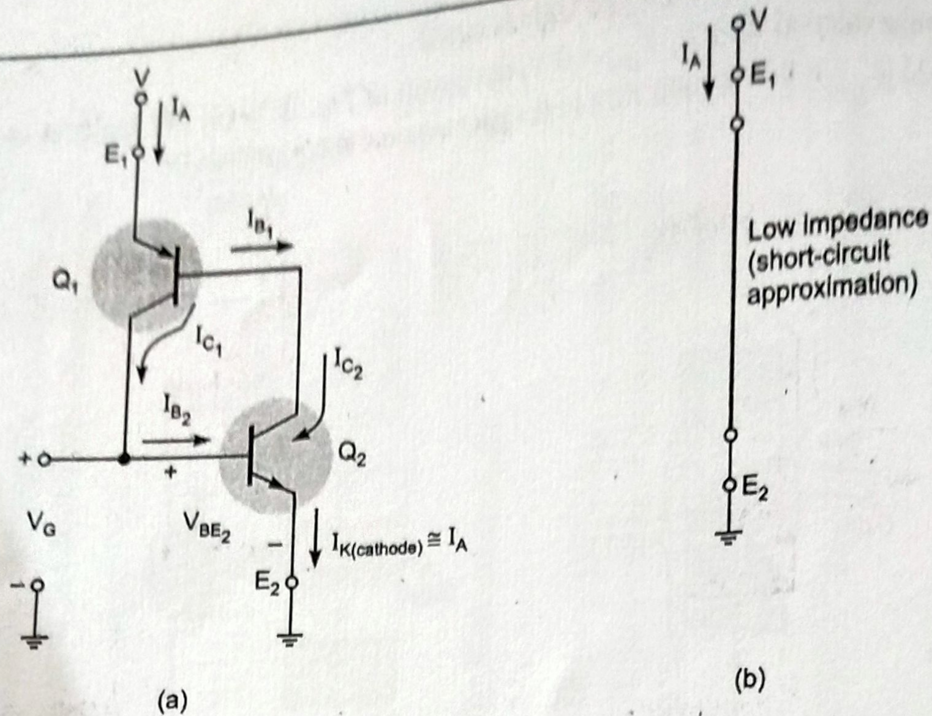


Fig. 38.32

- An SCR *cannot* be turned off by simply removing the gate signal. Only a special few can be turned off by applying a negative pulse to the gate terminal at $t = t_3$ [Fig. 38.31 (*a*)].

Volt-ampere (V - I) characteristics of an SCR

The characteristics of an SCR are provided in Fig. 38.33 for various values of gate current. It is the graph drawn between anode - cathode voltage (supply voltage) V_F and the anode current I_A for various values of gate current I_G.

(*i*) Forward characteristics:

- As the supply voltage increases, the anode current remains very small at first and SCR is in the "OFF" state.
- As the supply voltage increases further, the anode current also increases. At a particular voltage ($V_{(BR)F^*}$), called *Forward breakover voltage,* SCR is turned "ON" (fired). SCR conducts heavy current.

1. *Forward breakover voltage* $V_{(BR)F^*}$ is the voltage above which the SCR enters the conduction region. The asterisk (*) denotes the letter to be added, which is dependent on the condition of the gate terminal as follows:

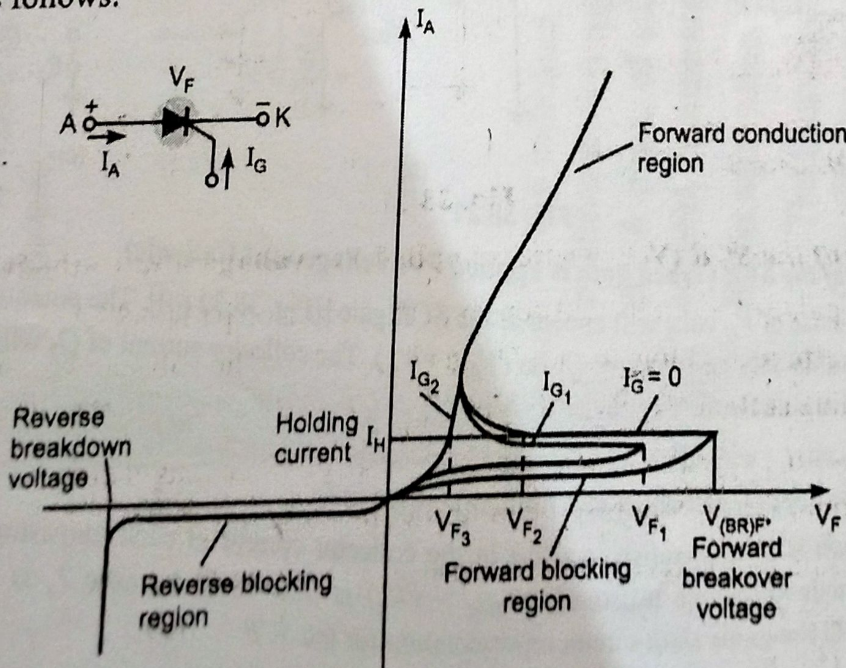


Fig. 38.33

O = open circuit from G to K

S = short circuit from G to K

R = resistor from G to K

V = fixed bias (voltage) from G to K

2. *Holding current* I_H is the value of current below which the *SCR* switches from the ...uction state to the forward blocking region under stated conditions.

3. *Forward blocking region* is the region corresponding to the open-circuit condition for the ...olled rectifier that *blocks* the flow of charge (current) from anode to cathode.

...ves for varying values of I_G

- For the characteristic having $I_G = 0$, V_F must reach the largest required breakover voltage ($V_{(BR)F^*}$) before the "collapsing" effect results and the SCR can enter the conduction region corresponding to the *on* state.
- If the gate current is increased to I_{G1}, by applying a bias voltage to the gate terminal, the value of V_F required for the conduction (V_{F1}) is considerably less. Note also that I_H drops with increase in I_G.
- If the gate current is increased to I_{G2}, the *SCR* will fire at very low values of voltage (V_{F3}). The characteristics will begin to approach those of the basic *p–n* junction diode.

***(ii)* Reverse characteristics:**

When anode is given negative voltage w.r.t cathode, the curve between voltage and current is ...wn as reverse characteristic.

- As the reverse voltage increases, the increase in anode current is very small. At a particular reverse voltage, avalanche breakdown occurs and SCR conducts heavily in the reverse direction. This maximum reverse voltage at which SCR starts conducting heavily is known as *"reverse breakover voltage"*.

  Reverse breakdown voltage is equivalent to the Zener or avalanche region of the fundamental ...-layer semiconductor diode.

- *Reverse blocking region* is the region correponding to the open-circuit condition for the controlled rectifier that *blocks* the flow of charge (current) from anode to cathode.

38.11 SCR APPLICATIONS

Series Static Switch :

Fig. 38.34 shows a half wave *series static switch.*

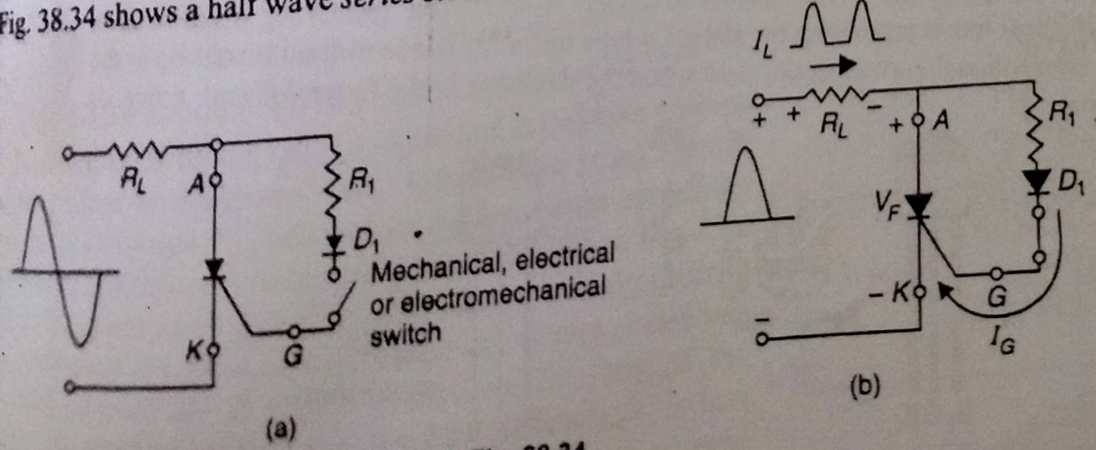


Fig. 38.34

If the switch is closed as shown in Fig. 38.34 (*b*), a gate current will flow during the positive ...tion of the input signal, turning the SCR on. Resistor R_1 limits the magnitude of the gate current.

Average output voltage,

$$V_{av} = \frac{1}{\pi}\int_{\alpha}^{180°} V_m \sin\theta \, d\theta = \frac{V_m}{\pi}[\cos\alpha - \cos 180°] = \frac{V_m}{\pi}(1 + \cos\alpha)$$

∴ Average current, $I_{av} = \dfrac{V_{av}}{R_L} = \dfrac{V_m}{\pi R_L}(1 + \cos\alpha)$

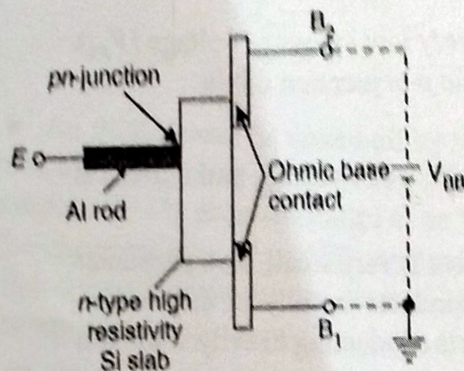
Thus I_{av} in full wave rectifier is two times that of half wave rectifier.

UNIJUNCTION TRANSISTOR (UJT)

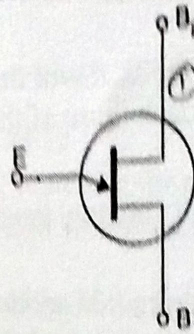
38.12 UNIJUNCTION TRANSISTOR (UJT)

Construction

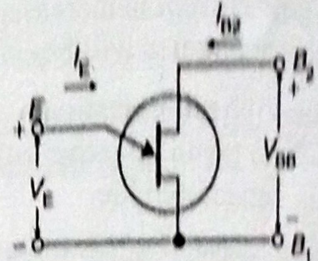
Fig. 38.37 (*a*) shows the basic construction of a unijunction transistor (UJT).



(*a*) Basic construction of a UJT



(*b*) Symbolic representation

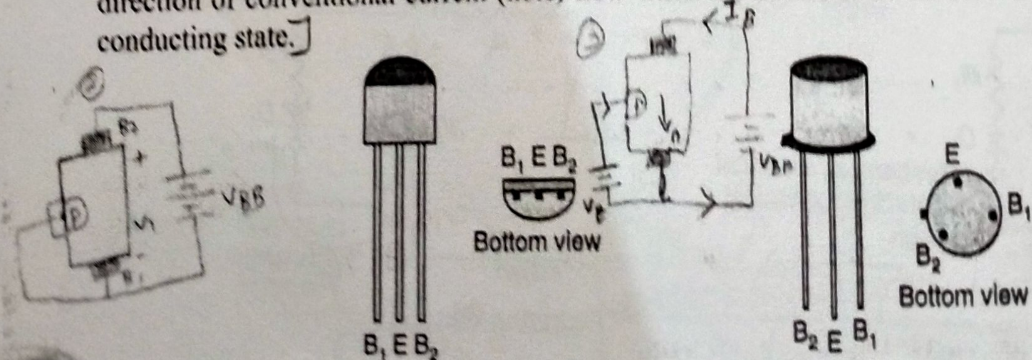


(*c*) Biasing arrangement

Fig. 38.37

It is a three-terminal device. A slab of lightly doped (increased resistance characteristic) *n*-type silicon material has two base contacts attached to both ends of one surface and an aluminium rod alloyed to the opposite surface. The *p-n* junction of the device is formed at the boundary of the aluminium rod and the *n*-type silicon slab. The single *p-n* junction accounts for the terminology *unijunction*. The aluminium rod is alloyed to the silicon slab at a point closer to the base 2 contact than the base 1 contact. Further, base 2 terminal is made positive with respect to the base 1 terminal by V_{BB} volts.

Fig. 38.37 (*b*) shows the circuit symbol of a UJT. Note that the emitter leg is drawn at an angle to the vertical line representing the slab of *n*-type material. The arrowhead is pointing in the direction of conventional current (hole) flow when the device is in the forward-biased, active, or conducting state.



(a) Resin-encapsulated UJT

(b) UJT in a metal can

The basic biasing arrangement for the unijunction transistor is provided in Fig. 38.37 (*c*).

Equivalent Circuit of a UJT

The circuit equivalent of the UJT is shown in Fig. 38.38. Note the relative simplicity of this equivalent circuit: two resistors (one fixed, one variable) and a single diode.

The resistance of the silicon bar is represented by two series resistors: R_{B_2} is the resistance of the base-2 portion.

The resistance R_{B_1} is shown as a variable resistor since its magnitude will vary with the current I_E. For a representative UJT, R_{B_1} may vary from 5 kΩ down to 50 Ω for a corresponding change of I_E from 0 to 50 μA.

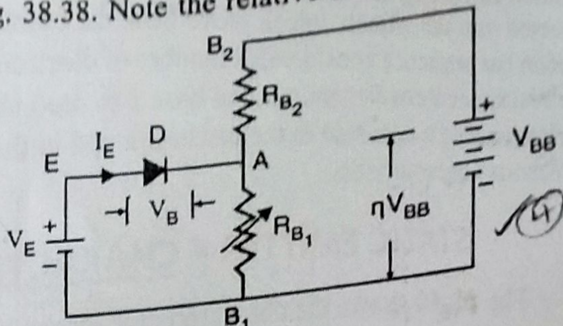


Fig. 38.38

The interbase resistance R_{BB} is the resistance between terminals B_1 and B_2 when $I_E = 0$. In equation form,

$$R_{BB} = (R_{B_1} + R_{B_2})\big|_{I_E=0} \quad ...(1)$$

Typically, R_{BB} ranges from 4 to 10 kΩ.

The position of the aluminium rod will determine the relative values of R_{B_1} and R_{B_2} with $I_E = 0$.

A battery V_{BB} is connected across $B_2\,B_1$ of equivalent circuit of UJT. Part of V_{BB} is dropped over R_{B2} and part on R_{B1}.

The magnitude of V_{RB_1} (with $I_E = 0$ *i.e.*, emitter open) is determined by the voltage-divider rule.

$$V_{RB_1} = \frac{R_{B_1}\,V_{BB}}{R_{B_1} + R_{B_2}} = \eta V_{BB}\bigg|_{I_E=0} \quad ...(2)$$

Here, η is called the *intrinsic stand-off ratio* of the device. It is defined by

$$\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}\bigg|_{I_E=0} = \frac{R_{B_1}}{R_{BB}} \quad ...(3)$$

For applied emitter potentials (V_E) greater than $V_{RB_1} (= \eta V_{BB})$ by the forward voltage drop of the diode V_D (0.35 → 0.70 *V*), the diode will fire. Assume the short-circuit representation (on an ideal basis), and I_E will begin to flow through R_{B1}. In equation form, the emitter firing potential is given by

$$V_P = \eta\,V_{BB} + V_D \quad ...(4)$$

OPERATION OF UJT

Fig. 38.39 shows the basic circuit operation of UJT. Normally the base 1 (B_1) is grounded. A positive voltage V_{BB} is applied at the base 2 (B_2). When there is no emitter current, this voltage V_{BB} produces a uniform drop across the 5000 to 10,000 ohms internal resistance of silicon bar. The resultant current through the bar will produce a voltage drop ηV_{BB} between points *A* and B_1 of the bar where *A* denotes the point, where the *P* region is formed. So long as the voltage V_E applied to the emitter with respect to B_1 is less than V_A or $V_P (= \eta\ V_{BB})$, the *p-n* junction remains reverse

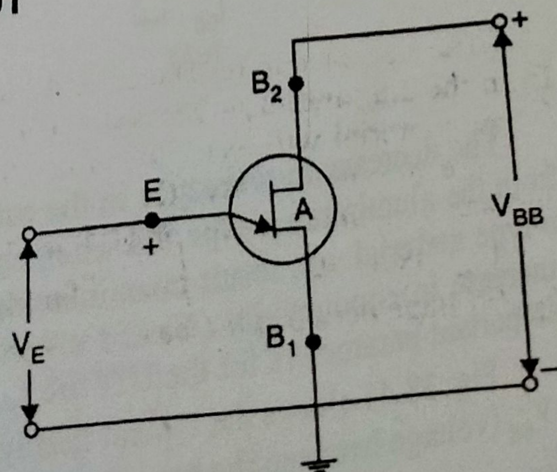


Fig. 38.39

biased and only a very small reverse current I_E flows in the emitter circuit. However, at the instant the emitter voltage V_E becomes greater than ηV_{BB}, the junction becomes forward biased and the emitter current I_E increases. The increase is quite steep because this current is due to the holes injected into the silicon, which move from the emitter to base 1. The presence of these holes in the silicon bar attracts a considerable number of electrons to this region and, in consequence, causes the bar resistance between emitter and base 1 to drop sharply. The upshot is that an increase in emitter current causes a decrease in the resistance and in the emitter voltage, which is known as a negative resistance characteristic.

STATIC EMITTER – CHARACTERISTIC CURVE FOR A UJT

Fig. 38.40 shows the characteristics of a representative unijunction transistor for $V_{BB} = 10$ V.

If V_{BB} is made zero, and a voltage is applied to V_E, the resulting current I_E that flows gives the emitter to base-1 diode characteristic ($I_{B2} = 0$).

Note that for emitter potentials to the left of the peak point, the magnitude of I_E is never greater than I_{E0} (measured in microamperes). The current I_{E0} corresponds very closely with the reverse leakage current I_{C0} of the conventional bipolar transistor. This region, is called the *cut off region*. Conduction is established at $V_E = V_P$. After V_P, an attempt to increase V_E is followed by a sudden increase in emitter current I_E with a corresponding decrease in V_E. This corresponds to a *negative resistance* region. After the negative resistance region, the valley point is reached. Further increase in I_E places the device in the *saturation region* (with characteristic approaching that of a semiconductor diode).

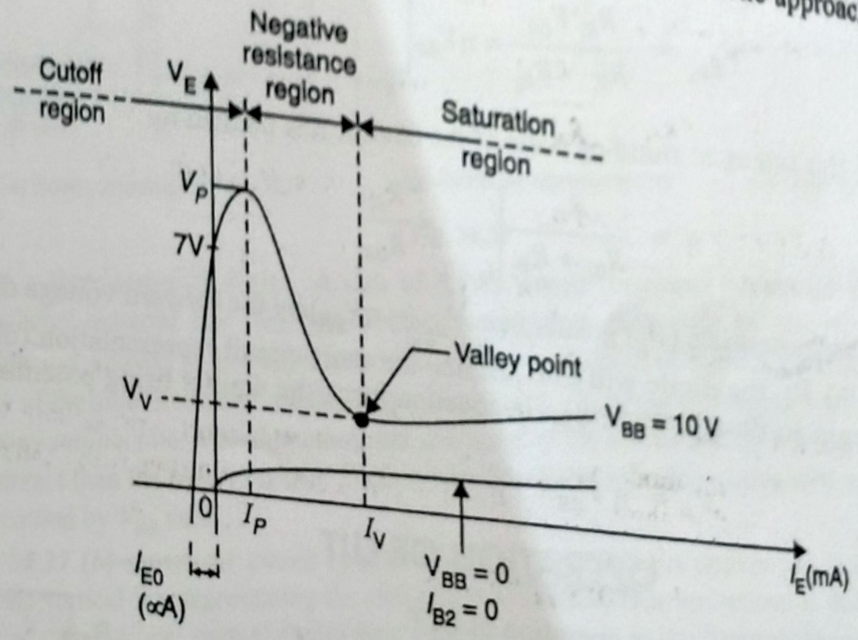


Fig. 38.40

The decrease in resistance in the active region is due to the holes injected into the *n*-type slab from the aluminium *p*-type rod when conduction is established. The increased hole content in the *n*-type material will result in an increase in the number of free electrons in the slab, producing an increase in conductivity (G) and a corresponding drop in resistance ($R \downarrow = 1/G \uparrow$). Three other important parameters for the UJT are I_P, V_V and I_V. Each is indicated on Fig. 38.40.

Fig. 38.41 shows the typical family of *static emitter characteristic curves* of a UJT for various V_{BB} (voltage between the bases) values.

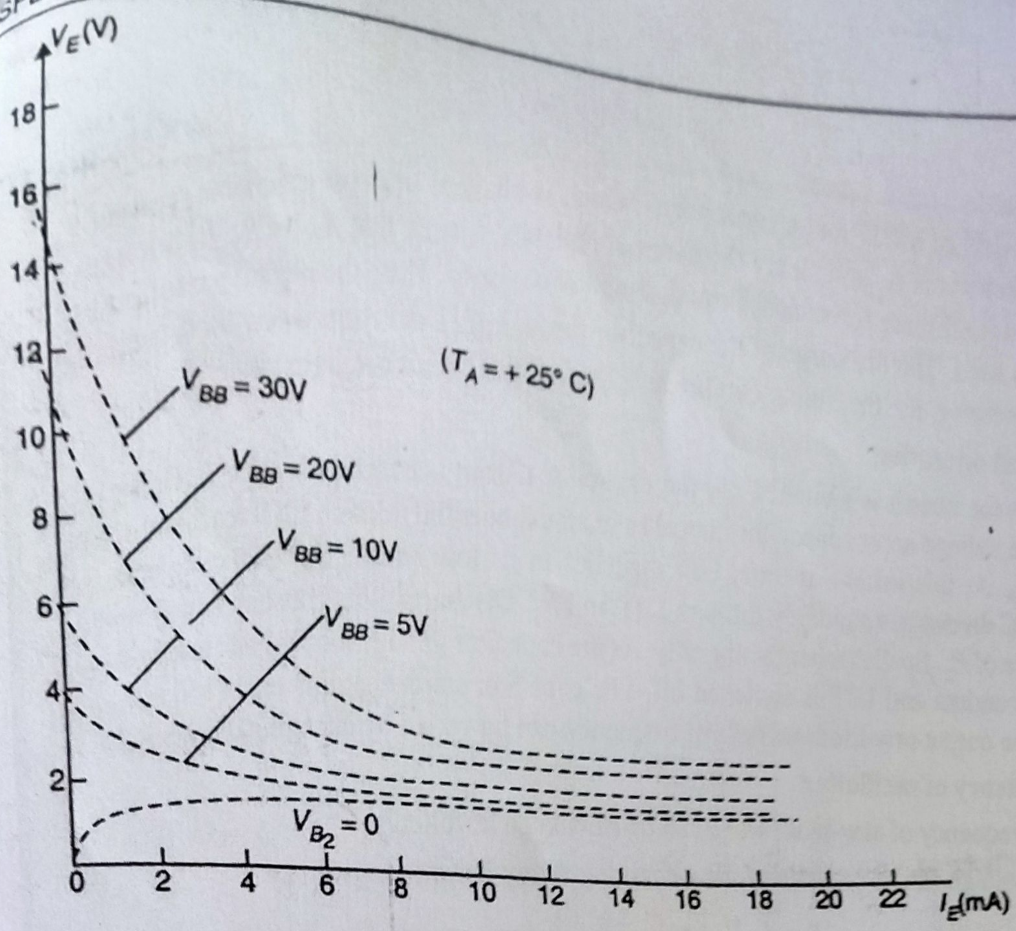


Fig. 38.41

Note that I_{E0} (μA) is not in evidence since the horizontal scale is in milliamperes.

The intersection of each curve with the vertical axis is the corresponding value of V_P. For fixed values of η and V_D, the magnitude of V_P will vary as V_{BB}, that is,

$$V_P \uparrow = \eta V_{BB} \uparrow + V_D$$

fixed

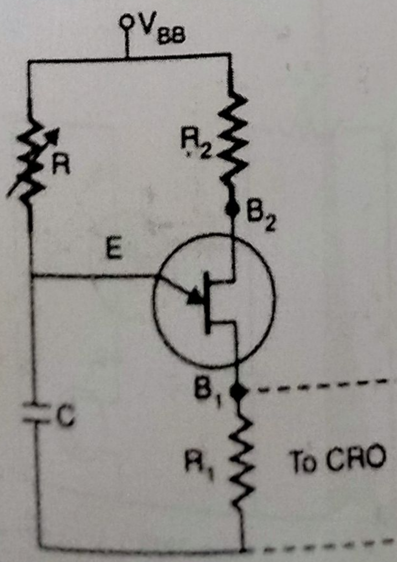
38.13 APPLICATIONS OF UJT

(1) UJT relaxation oscillator

The UJT can be used in a single stage oscillator circuit to provide a pulse signal suitable for digital-circuit applications.

Circuit Details

Fig. 38.42 shows the circuit of the UJT relaxation oscillator.



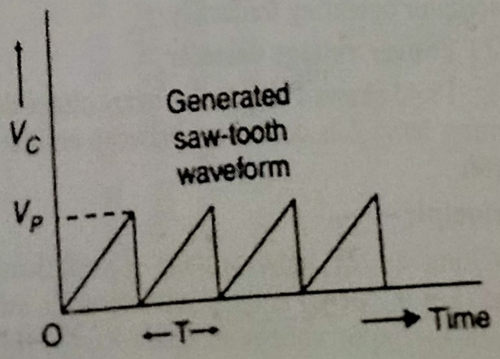


Fig. 38.42

It consists of a UJT and a capacitor C which is charged through a variable resistance R when V_{BB} is switched on. R_1 and R_2 are the external resistances such that $R_1 << R_2$. R_1 is less than 50 Ω. The inclusion of these resistances provide spike waveforms. Here the negative resistance region of the UJT is used. The discharge of the capacitor through UJT develops a saw-tooth output. Resistor R and capacitor C are the timing components that set the circuit oscillating rate.

Circuit operation

When the circuit is switched on, the capacitor C starts charging through R. During charging period, the voltage across capacitor increases in an exponential relation till it reaches the peak point voltage V_P. At this instant of time, UJT switches to its low resistance conducting mode. So, the capacitor C discharges suddenly through UJT and R_1. Discharge time constant is very small due to small value of R_1. So C discharges abruptly. As the capacitor voltage moves back to zero, the emitter ceases to conduct and UJT is switched off. The capacitor starts charging again and the next cycle begins. The output saw-tooth waveform frequency can be varied by changing the value of R.

Frequency of oscillation

The frequency of saw-tooth wave can be calculated as follows :

The voltage across capacitor during charging at any instant t is given by

$$v_c = V_{BB}(1 - e^{-t/\tau})$$

where τ is charging time constant = RC.

This voltage is applied to the emitter. So

$$v_c = V_E = V_{BB}(1 - e^{-t/\tau})$$

When capacitor charges to peak voltage V_P, UJT triggers. The UJT triggers when $V_P = \eta V_{BB}$.

If the capacitor takes a time T to charge to firing potential V_P, then

$$V_P = V_{BB}(1 - e^{-T/CR})$$

or

$$\frac{V_P}{V_{BB}} = \eta = (1 - e^{-T/CR})$$

or

$$e^{-T/CR} = 1 - \eta$$

or

$$T = CR \log_e\left(\frac{1}{1-\eta}\right)$$

Frequency of oscillation, $f = \dfrac{1}{T} = \dfrac{1}{RC \log_e\left(\dfrac{1}{1-\eta}\right)}$.

The oscillating frequency may be calculated using the above equation, which includes the UJT intrinsic stand-off ratio η as a factor (in addition to R and C) in the oscillator operating frequency.

(2) UJT as over voltage detector

Fig. 38.43 shows a simple d.c. over voltage detector. A warning lamp L is connected between emitter E and B_1 circuit.

Principle

As long as the input voltage is less than peak-point voltage V_P of UJT, the device remains switched off. When the input voltage exceeds V_P, the device is switched on.

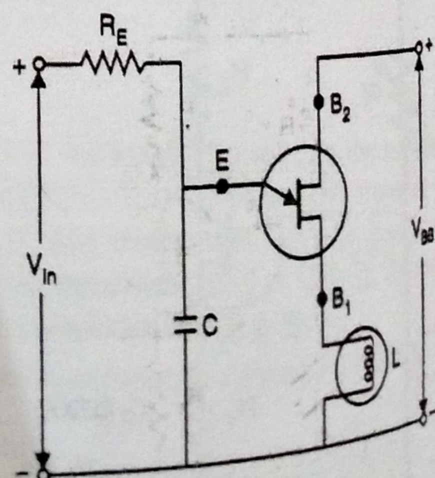


Fig. 38.43

20.5 V-I Characteristics of SCR

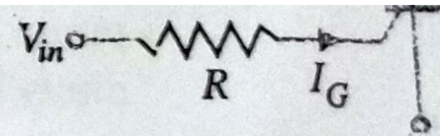


Fig. 20.6

It is the curve between anode-cathode voltage (V) and anode current (I) of an *SCR* at constant gate current. Fig. 20.7 shows the *V-I* characteristics of a typical *SCR*.

(*i*) **Forward characteristics.** When anode is positive *w.r.t.* cathode, the curve between V and I is called the forward characteristic. In Fig. 20.7, *OABC* is the forward characteristic of *SCR* at $I_G = 0$. If the supply voltage is increased from zero, a point is reached (point *A*) when the *SCR* starts conducting. Under this condition, the voltage across *SCR* suddenly drops as shown by dotted curve *AB* and most of supply voltage appears across the load resistance R_L. If proper gate current is made to flow, *SCR* can close at much smaller supply voltage.

(*ii*) **Reverse characteristics.** When anode is negative *w.r.t.* cathode, the curve between V and I is known as *reverse characteristic.* The reverse voltage does come across *SCR* when it is operated with a.c. supply. If the reverse voltage is gradually increased, at first the anode current remains small (*i.e.* leakage current) and at some reverse voltage, avalanche breakdown occurs and the *SCR* starts conducting heavily in the reverse direction as shown by the curve *DE*. This maximum reverse voltage at which *SCR* starts conducting heavily is known as *reverse breakdown voltage.*

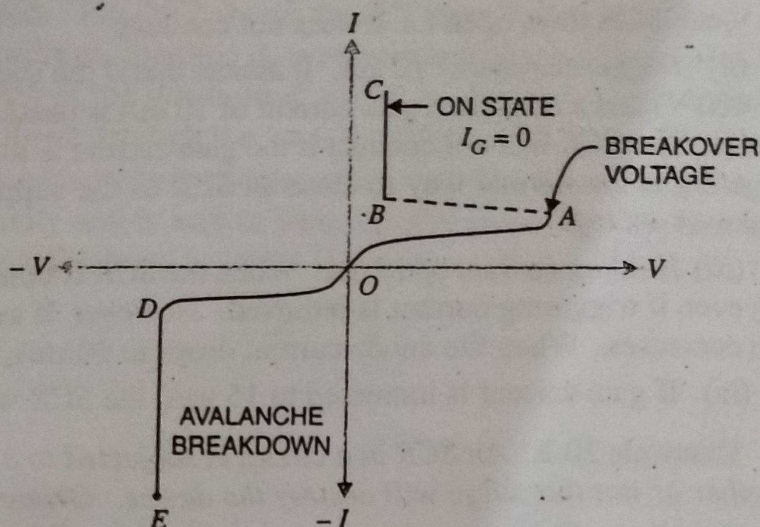


Fig. 20.7

20.6 SCR in Normal Operation

In order to operate the *SCR* in normal operation, the following points are kept in view :

(i) The supply voltage is generally much less than breakover voltage.

(ii) The *SCR* is turned on by passing an appropriate amount of gate current (a few mA) and not by breakover voltage.

(iii) When *SCR* is operated from a.c. supply, the peak reverse voltage which comes during negative half-cycle should not exceed the reverse breakdown voltage.

(iv) When *SCR* is to be turned *OFF* from the *ON* state, anode current should be reduced to holding current.

(v) If gate current is increased above the required value, the *SCR* will close at much reduced supply voltage.

20.7 SCR as a Switch

The *SCR* has only two states, namely; *ON* state and *OFF* state and no state inbetween. When appropriate gate current is passed, the *SCR* starts conducting heavily and remains in this position indefinitely even if gate voltage is removed. This corresponds to the *ON* condition. However, when the anode current is reduced to the holding current, the *SCR* is turned *OFF*. It is clear that behaviour of *SCR* is similar to a mechanical switch. As *SCR* is an electronic device, therefore, it is more appropriate to call it an *electronic switch*.

Advantages of SCR as a switch. An *SCR* has the following advantages over a mechanical or electromechanical switch (relay) :

(i) It has no moving parts. Consequently, it gives noiseless operation at high efficiency.

(ii) The switching speed is very high upto 10^9 operations per second.

(iii) It permits control over large current (30–100 A) in the load by means of a small gate current (a few mA).

(iv) It has small size and gives trouble free service.